

## ANTIOPE TIMING CHAIN CIRCUIT FOR U.S.A. 525 LINE SYSTEM

The SAA5125 is an N-channel MOS integrated circuit which provides the necessary timing control signals for a full Antiope/Titan decoder system, in a 28-lead DIL encapsulation. The circuit controls the addressing of the page memory to produce a television display of 40 characters by 21 rows for the 525 line U.S.A. standard.

### Features

- Fully functional operation over the supply voltage range of 4.5 to 5.5 V and ambient temperature range  $-20$  to  $70^{\circ}\text{C}$ .
- Supply voltage pin ( $V_{DD}$ ) and all input pins are rated to withstand voltages in the range  $-0.3$  to  $7.5$  V (maximum).
- F6 input clamp available if a.c. coupling is used.
- Outputs in high impedance rated for  $-0.3$  to  $7.5$  V (maximum).
- Open drain outputs rated for  $-0.3$  to  $13.2$  V (maximum).
- Electrostatic protection on all inputs and outputs up to  $1000$  V.

### QUICK REFERENCE DATA

$V_{DD} = 5$  V;  $V_{SS} = 0$  V;  $T_{amb} = 25^{\circ}\text{C}$ ; F6 = 6.0419 MHz

|                                     |              | min. | typ. | max.  |               |
|-------------------------------------|--------------|------|------|-------|---------------|
| Operating supply voltage            | $V_{DD}$     | 4.5  | —    | 5.5   | V             |
| Operating supply current            | $I_{DD}$     | —    | 25   | —     | mA            |
| Input voltage LOW                   | $V_{IL}$     | —    | —    | 0.8   | V             |
| Input voltage LOW, F6 only (note 1) | $V_{IL}$     | —    | —    | 0.8   | V             |
| Input voltage HIGH                  | $V_{IH}$     | 2.0  | —    | 5.5   | V             |
| Input voltage HIGH, F6 only         | $V_{IH}$     | 2.7  | —    | 6.5   | V             |
| Input leakage current               | $\pm I_{IR}$ | —    | —    | 10    | $\mu\text{A}$ |
| F6 mark to space ratio              |              | —    | —    | 56:44 |               |

Output currents are given with pin descriptions

note 1 Input voltage can be negative if a.c. coupling is used.

### PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117)

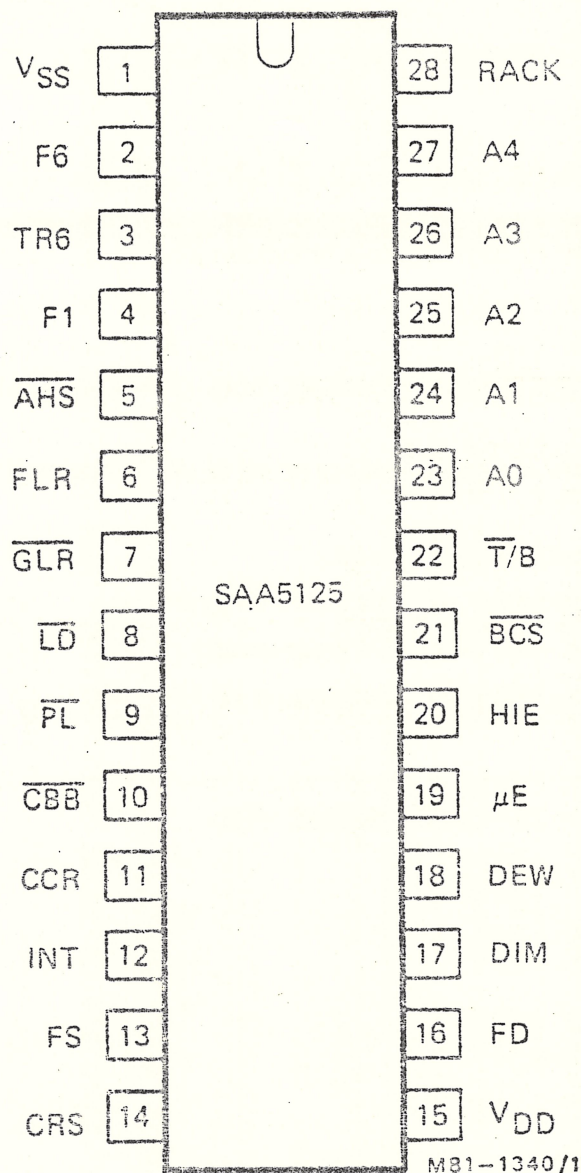


Fig.1 Pinning diagram

## PIN DESCRIPTION

Pin number

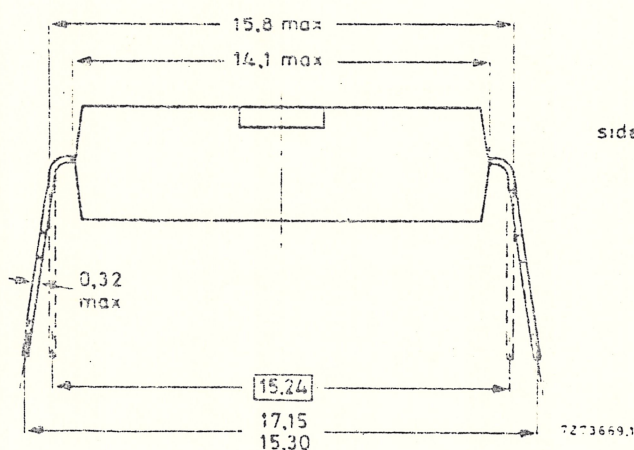
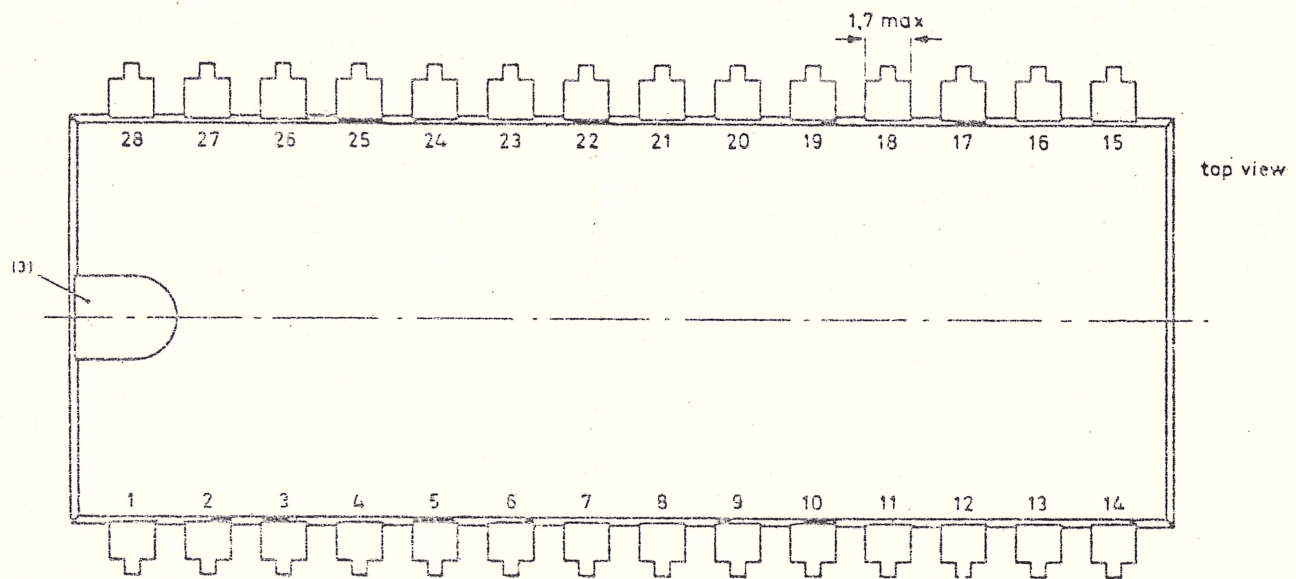
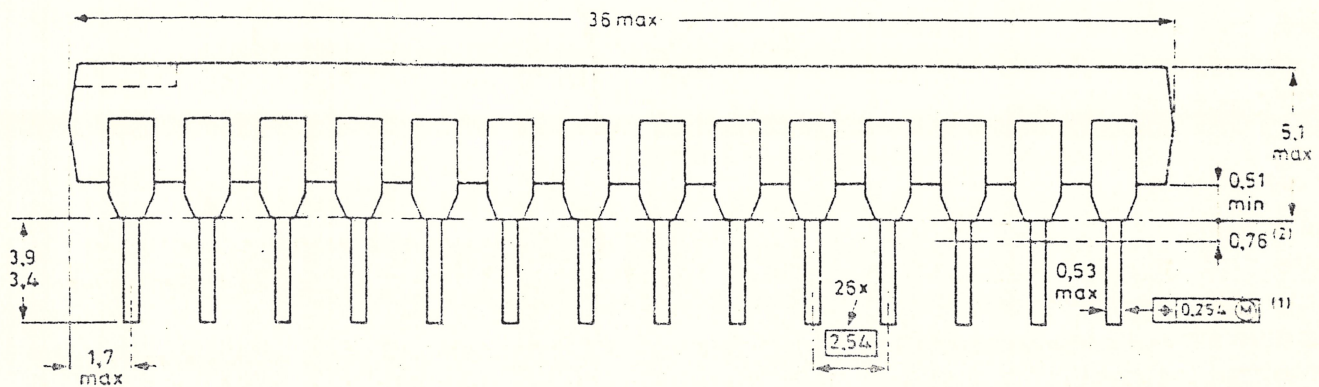
1. V<sub>SS</sub> Ground (0 V)
2. F6 6.0419 MHz input
3. TR6 6.0419 MHz push-pull clock output (-I<sub>OH</sub> = 100 μA; I<sub>OL</sub> = 100 μA)
4. F1 1.007 MHz push-pull clock output (-I<sub>OH</sub> = 200 μA; I<sub>OL</sub> = 200 μA)
5. AHS After hours sync push-pull output (-I<sub>OH</sub> = 200 μA; I<sub>OL</sub> = 1.6 mA)
6. FLR Fast line reset input
7. GLR General line reset push-pull output (-I<sub>OH</sub> = 200 μA; I<sub>OL</sub> = 1.6 mA)
8. LD Line drive open drain output (I<sub>OL</sub> = 1.6 mA)
9. PL Phase lock open drain output (I<sub>OL</sub> = 2 mA)

10.  $\overline{\text{CBB}}$  Colour burst blanking open drain output ( $I_{OL} = 2 \text{ mA}$ )
11. CCR Column counter reset push-pull output ( $-I_{OH} = 200 \mu\text{A}$ ;  $I_{OL} = 1.6 \text{ mA}$ )
12. INT Interlace mode input
13. FS Field sync input
14. CRS Character rounding select push-pull output ( $-I_{OH} = 200 \mu\text{A}$ ;  $I_{OL} = 1.6 \text{ mA}$ )
15.  $V_{DD}$  Supply voltage
16. FD Field drive open drain output ( $I_{OL} = 1.6 \text{ mA}$ )
17. DIM Displaying memory push-pull output ( $-I_{OH} = 100 \mu\text{A}$ ;  $I_{OL} = 1.6 \text{ mA}$ )
18. DEW Data entry window push-pull output ( $-I_{OH} = 200 \mu\text{A}$ ;  $I_{OL} = 1.6 \text{ mA}$ )
19.  $\mu\text{E}$  Microprocessor enable push-pull output ( $-I_{OH} = 100 \mu\text{A}$ ;  $I_{OL} = 1 \text{ mA}$ )
20.  $\overline{\text{HIE}}$  High impedance enable input
21.  $\overline{\text{BCS}}$  Big character select input
22.  $\overline{\text{T/B}}$  Top/Bottom input
- 23  
to 27 A0 to A4 Three state outputs: memory row address ( $-I_{OH} = 200 \mu\text{A}$ ;  $I_{OL} = 1.6 \text{ mA}$ )
28. RACK Read address clock push-pull output ( $-I_{OH} = 100 \mu\text{A}$ ;  $I_{OL} = 1.6 \text{ mA}$ )

DEVELOPMENT SAMPLE DATA



# 28-PIN DUAL IN-LINE; PLASTIC (SOT-117)



## Dimensions in mm

- ⊕ Positional accuracy.
- Ⓜ Maximum Material Condition.

- (1) Centre-lines of all leads are within  $\pm 0,127$  mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by  $\pm 0,254$  mm.
- (2) Lead spacing tolerances apply from seating plane to the line indicated.
- (3) Index may be horizontal as shown, or vertical.

## SOLDERING

### 1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).

If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

### 2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

### 3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

