National Semiconductor

LM1889 TV Video Modulator

General Description

The LM1889 is designed to interface audio, color difference, and luminance signals to the antenna terminals of a TV receiver. It consists of a sound subcarrier oscillator, chroma subcarrier oscillator, quadrature chroma modulators, and RF oscillators and modulators for two low-VHF channels.

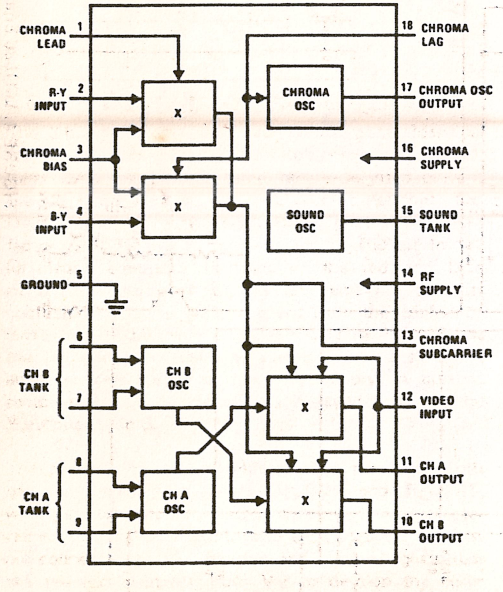
The LM1889 allows video information from VTR's, games, test equipment, or similar sources to be displayed on black and white or color TV receivers. When used with the MM57100 and MM53104, a complete TV game is formed.

Features

- dc channel switching
- 12V to 18V supply operation
- Excellent oscillator stability
- Low intermodulation products
- 5 Vp-p chroma reference signal
- May be used to encode composite video

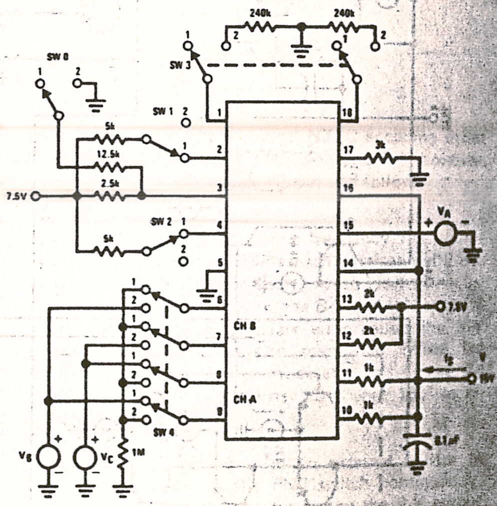
Block Diagram

Dual-In-Line Package



Order Number LM1889N
See NS Package N18A

DC Test Circuit



Absolute Maximum Ratings

Supply Voltage V14, V16 max	19 V_{dc}
Power Dissipation Package (Note 1)	1390 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Chroma Osc Current I_{17} max	10 mA_{dc}
(V16−V15) max	±5 V_{dc}
(V14−V10) max	7V
(V14−V11) max	7V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics (dc Test Circuit, All SW Normally Pos. 1, V_A = 15V, V_B = V_C = 12V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current, I_S		20	35	45	mA
Sound Oscillator, Current Change, ΔI_{15}	Change V_A From 12.5V to 17.5V	0.3	0.6	0.9	mA
Chroma Oscillator Balance, V17		9.5	11.0	12.5	V
Chroma Modulator Balance, V13		7.0	7.4	7.8	V
R-Y Modulator Output Level, $\Delta V13$	SW 3, Pos. 2, Change SW 1 From Pos. 1 to Pos. 2	0.6	0.9	1.2	V
B-Y Modulator Output Level, $\Delta V13$	SW 3, Pos. 2, Change SW 2 From Pos. 1 to Pos. 2	0.6	0.9	1.2	V
Chroma Modulator Conversion Ratio, $\Delta V13/\Delta V3$	SW 3, Pos. 2, Change SW 0 From Pos. 1 to Pos. 2. Divide $\Delta V13$ by $\Delta V3$	0.45	0.70	0.95	V/V
Ch A Oscillator "OFF" Voltage, V8, V9	SW 4, Pos. 2	0.5	1.5	3.0	V
Ch A Oscillator Current Level, I_9	V_B = 12V, V_C = 13V	2.5	3.5	5	mA
Ch B Oscillator "OFF" Voltage, V6, V7		0.5	1.5	3.0	V
Ch B Oscillator Current Level, I_6	SW 4, Pos. 2, V_B = 12V, V_C = 13V	2.5	3.5	5	mA
Ch A Modulator Conversion Ratio, $\Delta V11/(V13-V12)$	SW 1, SW 2, SW 3, Pos. 2, V_B = 12V, Change V_C From 13V to 11V For $\Delta V11$ Divide By V13−V12	0.35	0.55	0.75	V/V
Ch B Modulator Conversion Ratio, $\Delta V10/(V13-V12)$	All SW, Pos. 2, V_B = 12V, Change V_C From 13V to 11V Divide as Above	0.35	0.55	0.75	V/V

AC Electrical Characteristics (ac Test Circuit, V = 15V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Chroma Oscillator Output Level, V17	$C_{LOAD} \leq 20$ pF	4	5		Vp-p
Sound Carrier Oscillator Level, V15	Loaded by RC Coupling Network	2	3	4	Vp-p
RF Oscillator Level, V8, V9	Ch. Sw. Pos. 3, f = 61.25 MHz,	200	350		mV

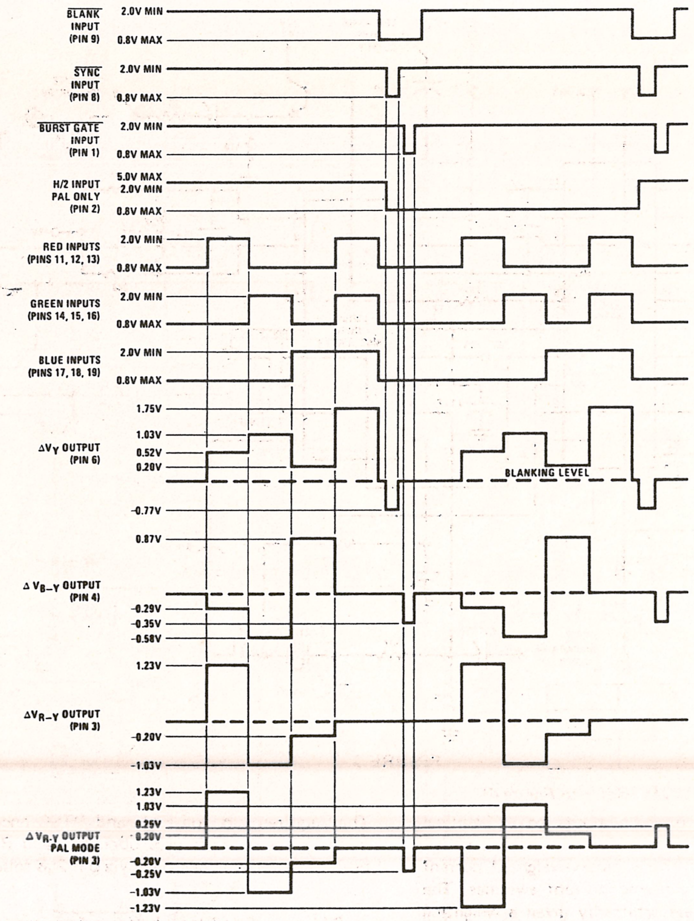
Absolute Maximum Ratings

Supply Voltage	
Pin 5	15V
Pin 20	6V
Input Voltage (Pins 1, 8, 9, 11–19)	–0.5V, +12V
Pin 2 Voltage Relative to Pin 20	0.8V
Output Current	5 mA
Power Dissipation, T_A = 25°C (Note 1)	1.67 W
Storage Temperature Range	–55°C to +150°C
Operating Temperature Range	0°C to 70°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics T_A = 25°C, (*Figure 2*, Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
5V Supply Current (Pin 20)	$\overline{BLANK}$ = 0.8V	7	11	16	mA
12V Supply Current (Pin 5)	$\overline{BLANK}$ = 0.8V	9	13	17	mA
Logic "1" Input Current (Pins 1, 2, 8, 9, 11–19)	Input Voltage = 5.0V		0	10	µA
Logic "0" Input Current (Pins 1, 2, 8, 9, 11–19)	Input Voltage = 0.3V		–0.01	–0.18	mA
Output Offsets	R, G, B = 0.8V				
ΔV_Y			0	±50	mV
$\Delta V_{R\text{-}Y}$			0	±50	mV
$\Delta V_{B\text{-}Y}$			0	±50	mV
R-Y Full Scale, $(\Delta V_{R\text{-}Y})_{FS}$	R = 2V; G, B = 0.8V	1.0	1.23	1.4	V
B-Y Full Scale, $(\Delta V_{B\text{-}Y})_{FS}$	B = 2V; R, G = 0.8V	0.7	0.87	1.0	V
Green Full Scale	G = 2V: R, B = 0.8V				
$\Delta V_{R\text{-}Y}$		–0.85	–1.03	–1.2	V
$\Delta V_{B\text{-}Y}$		–0.45	–0.58	–0.7	V
Y Full Scale	R, G, B = 2V				
$(\Delta V_Y)_{FS}$		1.6	1.75	1.9	V
$\Delta V_{R\text{-}Y}$			0	±100	mV
$\Delta V_{B\text{-}Y}$			0	±75	mV
O Carrier Reference, ΔV_O		2.0	2.2	2.5	V
Blanking Level, ΔV_Y	$\overline{BLANK}$ = 0.8V		0	±50	mV
Sync Level, ΔV_Y	$\overline{BLANK}$, $\overline{SYNC}$ = 0.8V	–0.67	–0.77	–0.87	V
NTSC Burst, $\Delta V_{B\text{-}Y}$	$\overline{BLANK}$, $\overline{BURST\ GATE}$ = 0.8V	–0.26	–0.35	–0.46	V
PAL Burst					
$\Delta V_{R\text{-}Y}$	SW in PAL Position;	–0.2	–0.25	–0.32	V
$\Delta V_{B\text{-}Y}$	$\overline{BLANK}$, $\overline{BURST\ GATE}$, H/2 = 0.8V	–0.2	–0.25	–0.32	V
PAL Inversion Ratio $(\Delta V_{R\text{-}Y})_{PAL}/(\Delta V_{R\text{-}Y})_{FS}$	R = 2V; G, B, H/2 = 0.8V SW to PAL Position	–0.9	–1.0	–1.1	
Y Linearity Error	*Figure 2b* Input Connection		±1	±6	%FS
Y Switching Times	15 kHz Square Wave Switching R, G, B in Parallel				

Typical Input and Output Waveforms



Application Notes (Refer to *Figure 3*)

$\overline{SYNC}$, $\overline{BLANK}$, and $\overline{BURST\ GATE}$ may be obtained from a sync generator IC similar to MM5320 or MM5321. For PAL operation, the H/2 square wave may be obtained by a ÷2 from horizontal sync.

All inputs are low-power TTL compatible. Because of the very low typical input currents, the color inputs may be paralleled in various combinations. For simple color requirements, the *Figure 2a* input connection may be used to produce the 6 primary and complementary colors listed in Table I, along with black and white. To add complex colors such as those at the bottom of Table I, all 9 input bits may be required separately. When choosing input codes for other colors, always check the new color against both light and dark backgrounds.

TABLE I. INPUT CODE EXAMPLES FOR COMMON COLORS

		INPUT CODE								
		RED			GREEN			BLUE		
	COLOR	M		L	M		L	M		L
	Black	0	0	0	0	0	0	0	0	0
	Dark Grey	0	1	0	0	1	0	0	1	0
	Light Grey	1	0	1	1	0	1	1	0	1
	White	1	1	1	1	1	1	1	1	1
Primary	Red	1	1	1	0	0	0	0	0	0
Primary	Green	0	0	0	1	1	1	0	0	0
Primary	Blue	0	0	0	0	0	0	1	1	1
Complementary	Cyan	0	0	0	1	1	1	1	1	1
Complementary	Magenta	1	1	1	0	0	0	1	1	1
Complementary	Yellow	1	1	1	1	1	1	0	0	0

LM1886

Circuit Description (See Schematic Diagram)

The LM1880 uses a phase-shift type voltage-controlled oscillator (VCO). The gain for the oscillator loop is derived from differential amplifiers Q30, Q31 and Q22, Q23. The collector current in Q23 is phase-shifted 45° at pin 5 and summed with a portion of the current in Q22, controlled by differential amplifier Q20, Q21. The resulting output phase at pin 4 coupled through the ceramic resonator to pin 6 defines the oscillation frequency. Differential amplifier Q16, Q17, controlled by the pin 2 voltage, determines the current split in Q20 and Q21 and, consequently, the pin 4 phase and oscillation frequency. The multiple-emitter degeneration in Q17 compensates the resonator phase characteristic to produce a nearly linear VCO control curve.

The 503.5 kHz output of the VCO is taken from squaring amplifier Q32, Q33 through Q34 and Q35 to the I^2L ÷16 pre-scaler T0–T3. The $2f_H$ output is then divided again in T4 to produce the desired horizontal frequency at gate G8. The horizontal pre-driver section consists of Q3, Q4 and Q5, which produce an open-collector output square-wave at pin 8.

The $2f_H$ pre-scaler output also drives a data flip-flop which resets the vertical counter F1–F9. The data input of the reset flip-flop is controlled by the vertical sync from pin 10 subject to gates G3 and G5. After 510 $2f_H$ cycles following reset, vertical sync from Q1 and G4 is enabled by G3. A sync pulse received after this time initiates reset on the next $2f_H$ cycle. If no pulse is received after 542 cycles, G5 will initiate the reset process. A reset pulse from the counter is taken via G9 to the retrace timing section. SCR Q8, Q9 is normally ON, holding a capacitor on pin 11 near ground. During this time Q11 and Q12 are OFF, allowing the vertical ramp to form on pin 12. When the reset pulse is received, Q7 turns Q8, Q9 OFF and Q11, Q12 ON, discharging the vertical ramp for the duration of the retrace time. Retrace is completed when the pin 11 capacitor charges to the Q8 threshold, and the SCR again latches.

The remaining sections of the device are the horizontal phase detector and burst gate former. The balanced phase detector consists of comparator Q43, Q44 and current source Q39 gated by differential amplifier Q41, Q42. Negative horizontal sync pulses on pin 14 enable the comparator, and the flyback sawtooth on pin 1 switches the current from Q43 to Q44 based on the relative phase between the sync and sawtooth. Q44 takes a (−) current pulse from pin 2, while the pulse in Q43 is turned around in the current mirror Q45, Q46 and Q47 to produce a (+) current pulse at pin 2. These currents are then integrated by the external loop filter to control the VCO.

The flyback sawtooth also switches differential amplifier Q49, Q50, which activates the burst gate. During the first half of the flyback pulse Q49 will be ON, which turns Q51 and Q52 ON and clamps pin 13 near ground. The sawtooth switches Q49, Q51 and Q52 OFF at the peak of the flyback, releasing pin 13. In this manner, the second half of a flyback pulse fed to pin 13 can be used as a burst gate.

Q53, Q54 and Q55 form the active shunt regulator which holds the supply pin 9 at 8.7V typ.

National Semiconductor

LM1886 TV Video Matrix D to A

General Description

The LM1886 is a TV video matrix D to A converter which encodes luminance and color difference signals from 3-bit red, green and blue inputs. The luminance output is encoded from the NTSC equation Y = 0.3R + 0.59G + 0.11B and the R-Y and B-Y outputs are weighted to prevent over-modulation. A built-in R-Y and burst gate polarity switch allow European PAL compatible signals to be encoded. All output levels including an RF O Carrier Bias Voltage have been referenced to 5V for direct connection to the LM1889 TV video modulator. When used in combination with the LM1889 and a suitable sync generator, 3-bit R, G and B information may be encoded to both composite video and RF channel carrier.

Features

- Complete digital to RF encoding with LM1889
- 1-pin PAL/NTSC mode select
- True NTSC matrix
- 8 levels of grey scale
- Allows wide range of colorimetry
- Low power TTL inputs
- Wideband luminance output
- Weighted R-Y, B-Y outputs

Connection Diagram

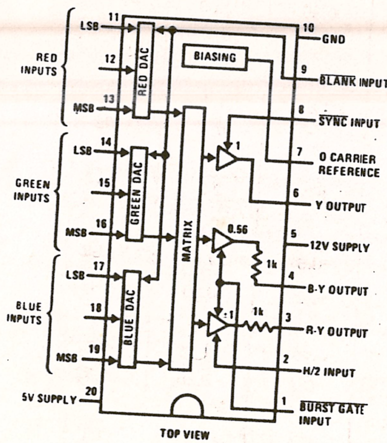


FIGURE 1

Order Number LM1886N
See NS Package N20A

Test Circuits

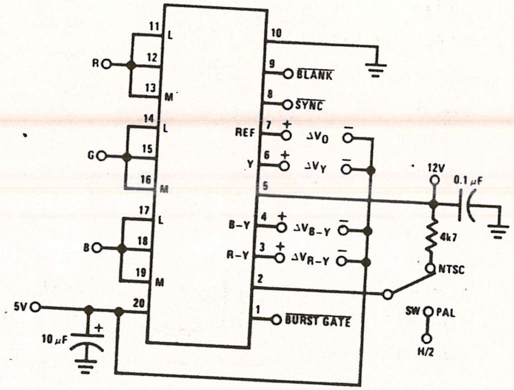


FIGURE 2a. 6-Color Input Connection