## VIDEO INTERFACE

| NAME | PIN TYPE | N° | FUNCTION | DESCRIPTION |
|---|---|---|---|---|
| R<br>G<br>B | O | 10<br>9<br>8 | Red<br>Green<br>Blue | These three TTL/LS compatible outputs deliver the video signal. They are low during the vertical and horizontal blanking intervals. |
| $\overline{TT}$ | O | 16 | Vertical synchronization | This TTL compatible output is active (low) for two lines each field period. The field period is programmable at 262 lines (60 Hz) or 312 lines (50 Hz). |
| TL | O | 25 | Horizontal synchronization | This TTL compatible output is at line frequency. It can be programmed active low for 4 window periods (for composite signal generation) or active high for 16 window periods (to directly drive a monitor). |
| I | O | 11 | Boxing command | This TTL/LS compatible output is active high. I allows to insert R,G,B in an external video signal for captioning purposes, for example. |
| SYT | I | 17 | Vertical synchronization input | This high impedance, high noise margin input is internally sampled and memorized on the 12 th window period of each line. When the memorized signal goes from high to low, the line count is reset at the end of the present line. This input allows to vertically synchronize VIN on an external composite or AC line signal. This input should be grounded if not used. |

## OTHER PINS

| | | | | |
|---|---|---|---|---|
| $V_{SS}$ | I | 4 | | This input has to be grounded. |
| CLK | I | 5 | Clock input | External TTL clock input. (nominal value : 3.5 MHz) |
| $\overline{VE}$ | I | 6 | VIN select | This TTL/MOS high impedance input must be wired to the corresponding GEN output. This input is active (low) each time the TB register of the mail box is accessed by the microprocessor. |
| C/$\overline{T}$ | I | 7 | Command or transfer select | This TTL/MOS high impedance input determines whether a command (C/$\overline{T}$ high) or data (C/$\overline{T}$ low) is accessed by the processor in the mail box. C/$\overline{T}$ is latched on the falling edge of $\overline{VE}$ and the request is memorized. |
| $\overline{RES}$ | I | 23 | Restart | When this TTL/MOS high impedance input goes low, the TL output goes high and remains in this state until the display mode register is loaded. |
| TST | I | 24 | Test | This pin must be grounded for normal operation. |
| $V_{CC}$ | S | 21 | Power supply | +5 V |
| GND | S | 1 | Power supply | Ground. |

## INTERNAL BUS CYCLES

The different types of internal bus cycles are given in the table below :

| CONTROL | | | | ADDRESS BUS AD (0 : 9) | DATA BUS A(0:7), B(0:7) | CYCLE TYPE |
|---|---|---|---|---|---|---|
| R/$\overline{W}$ | $\overline{SM}$ | $\overline{SG}$ | $\overline{ST}$ | | | |
| Read | Active | | | WINDOW ADDRESS (X', Y')<br>or CURSOR (X, Y) | MP → VIN, MP → CC | 1 |
| Read | | Active | | SLICE ADDRESS (NT') | GC or CC → VIN | 2 |
| Write | | | Active | – | T → VIN | 3 |
| Read | Active | | Active | CURSOR (X, Y) | MP → T | 4 |
| Write | Active | | Active | CURSOR (X, Y) | T → MP | 5 |
| Read | | Active | Active | SLICE ADDRESS (NT) | GC → T | 6 |
| Write | | Active | Active | SLICE ADDRESS (NT) | T → GC | 7 |

MP : Page Memory   T : Mail Box   GC : Character Generator   CC : Character Code Register

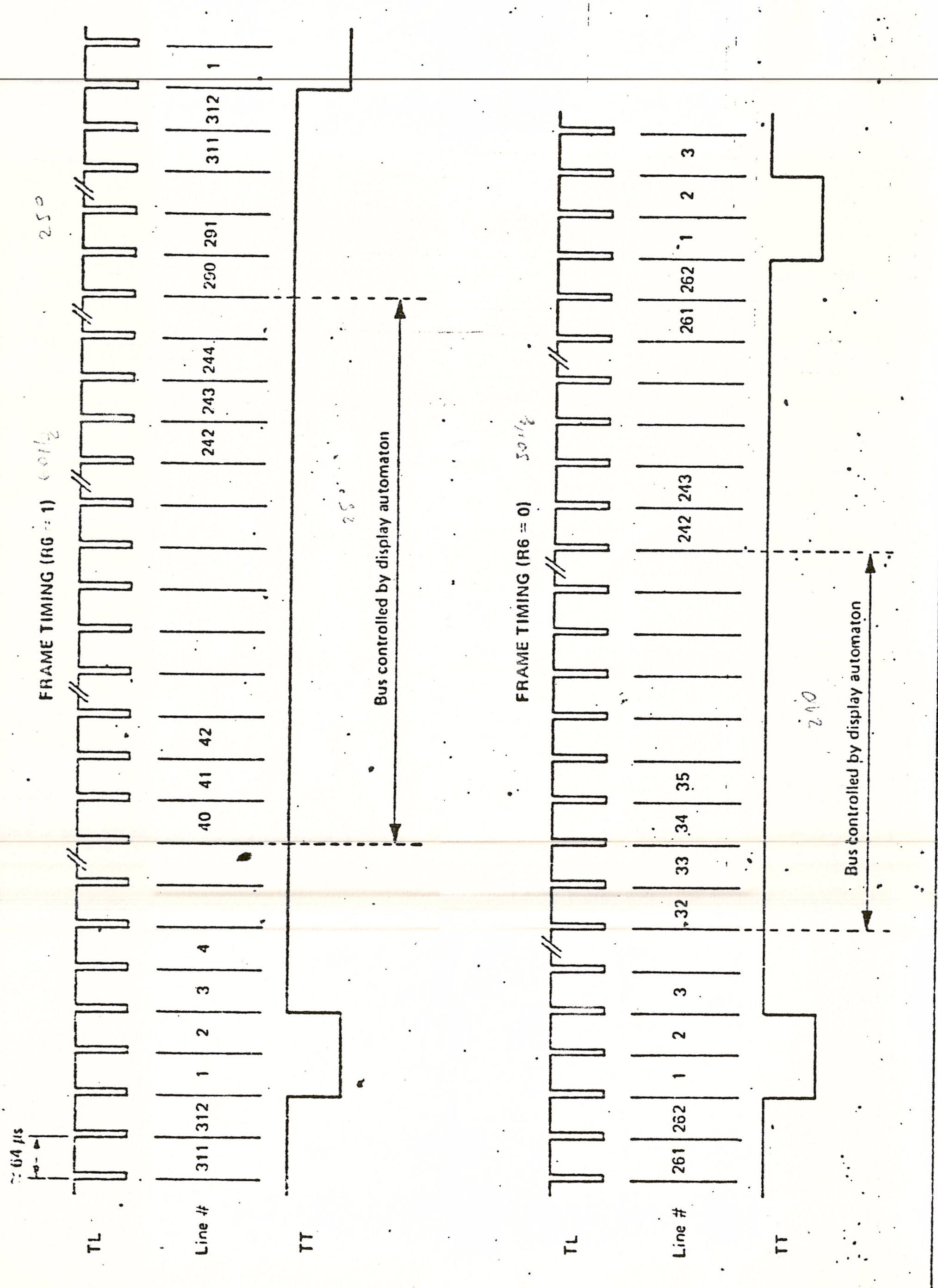
1, 2 : Used by display automaton
3 : Load command in access automaton
4 : Read MP
5 : Write MP
6 : Read Slice
7 : Write Slice

$\left.\begin{array}{l}4\\5\\6\\7\end{array}\right\}$ Controlled by access automaton

**NOTA :**
In cycle type 2, slice address is at ADR(0:3).
ADR4 gives the extension condition B7 ∧ (B5 ∨ B6) which has been latched on the previous type 1 cycle.
ADR(5:9) are not used.

In cycle types 6 and 7, slice address is at ADR(0:3). ADR4 gives the extension condition B7 ∧ (B5 ∨ B6) which has been latched on the previous type 1 cycle (with cursor address).

In cycle types 4 to 7, two strobes are simultaneously active. When a memory is read, T is written and reciprocally.








## GEN SIGNAL DESCRIPTION

GEN takes place in the video display unit between the internal 16 bit bus controlled by VIN and a general purpose 8 bit bus controlled by a processor. GEN contains :

- A character generator with 128 alphanumeric characters and 128 semigraphic characters.
- Two 8 bit registers - TA and TB - which perform as a mail box between the two buses.

### PROCESSOR INTERFACE

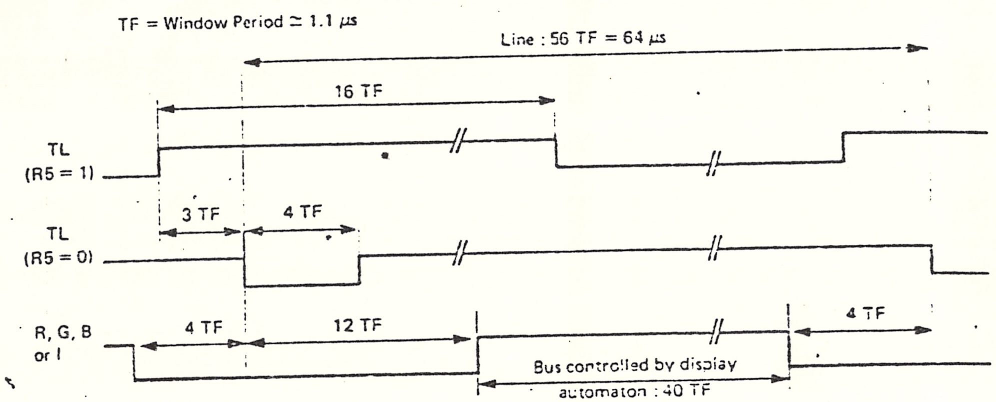
GEN interfaces to a processor bus on the bidirectional data bus D (0:7) using $\overline{CS}$, B/$\overline{A}$, C/$\overline{T}$, E and R/$\overline{W}$ as control signals.

| NAME | PIN TYPE | N° | FUNCTION | DESCRIPTION |
|---|---|---|---|---|
| D(0:7) | I/O | 32-25 | Data bus | The bidirectional data lines D(0:7) allow command and data transfer between the GEN internal mail box and the processor. Data bus output drivers are 3-state buffers which remain in the high impedance state except when the processor performs a display unit read operation. A high level on a data pin is a logical "1". |
| E | I | 20 | Enable | The enable signal is a high impedance TTL/MOS compatible input which enables the data bus input/output buffers and clocks data to and from the mail box. This signal is usually derived from the processor clock. |
| $\overline{CS}$ | I | 19 | Chip select | The $\overline{CS}$ line is a high impedance TTL/MOS compatible input which selects the display unit, when low, to read or write the internal mail box. |
| R/$\overline{W}$ | I | 23 | Read/Write | This high impedance TTL/MOS compatible input determines whether the internal mail box gets written or read. A write is active low ("0"). |
| B/$\overline{A}$ | I | 22 | Register TA or TB select | This high impedance TTL/MOS compatible input selects either the TA register (B/$\overline{A}$ = 0) or the TB register (B/$\overline{A}$ = 1) of the mail box. |
| C/$\overline{T}$ | I | 24 | Command or data transfer select | This high impedance TTL/MOS compatible input defines the contents of the mail box either as a command (C/$\overline{T}$ = 1) or as a data transfer (C/$\overline{T}$ = 0). The C/$\overline{T}$ input of GEN and the C/$\overline{T}$ input of VIN must be wired together for correct operations. |

VIN INTERFACE

| NAME | PIN TYPE | N° | FUNCTION | DESCRIPTION |
|---|---|---|---|---|
| $\overline{VE}$ | O | 18 | VIN select | This TTL compatible output must be wired to the corresponding VIN input. This signal goes active (low) when the TB register is accessed by the processor. |
| A(0:7)<br>B(0:7) | I/O | 33-40<br>16-9 | Internal data bus | These 16 bidirectional data lines allow data transfers between GEN, VIN and memory. |
| R/$\overline{W}$I<br>$\overline{SM}$<br>$\overline{SG}$<br>$\overline{ST}$ | I | 6<br>7<br>8<br>17 | Control signals from VIN | These inputs must be wired to the corresponding VIN outputs. |
| ADR(0:3) | I | 2-5 | Slice address | These four inputs must be wired to the corresponding four outputs of VIN. When $\overline{SG}$ is active, they are stable and determine the BCD address of a character slice in the character generator. |
| $V_{CC}$ | S | 21 | Power supply | +5 V |
| $V_{SS}$ | S | 1 | Power supply | Ground. |






262 line periods (if R6 = 0) or 312 line periods (if R6 = 1) make a frame period. The TT output is at frame period (60 Hz/50 Hz) and is low during 2 lines. SYT input resets the line count inside the frame : this input is triggered, then sampled when the 12th window of each line occurs. When the sample transits from 1 to 0, the line count will be reset on the next TL

### TIME SHARING OF THE BUS

When the display is enabled (R0 = 1), the timing generator gives control over the bus to the display automaton from the 40th line after TT to the 290th (if R6 = 1) or from the 32nd line to the 242nd (R6 = 0) and from the 13th to the 53rd window period of each line.

When the display is disabled (R0 = 0), the access automaton keeps control over the bus.

### READING WINDOW CODES AND CHARACTER SLICES

During each displayable window period (≃ 1.1 µs), the display automaton controls two read cycles on the internal bus.

On the first cycle, ADR(0:9) address a window code in the page memory.

The page memory is strobed by $\overline{SM}$ and a 16 bit window code is read (table 1).

The 11 bits of the attribute field A (0 : 6) and type field A7, B(5 : 7) are latched in the display automaton.

The 9 bits of the character code field A7, B(0 : 7) are latched in CC registers of the character generator.

CC register addresses one set of character and one character in the set.

A character is 10 slices of 8 bits each.

On the second cycle the slice number is given by ADR(0:3) and the extension select by ADR4. The character generator is strobed by $\overline{SG}$ and the value of the slice is read by the display automaton on the internal A(0:7) bus.

When a delimitor is addressed by CC, its contents is read in place of the value of the slice.

## DATA TRANSFERS ($C/\overline{T} = 0$)

When the mail box is written or read with $C/\overline{T} = 0$, the busy flip flop is set and GEN activates $\overline{VE}$. A data transfer request is memorized by the access automaton of VIN. As soon as the access automaton takes control over the internal bus, it executes the request according to the contents of the M register.

M(0 : 3) is a modulo 10 counter referred to as NT (slice number)

M(5 : 7) defines an access mode (see table 3).

### WRITE

It is the most commonly used data transfer : the contents of the mail box is written into the page memory location addressed by the cursor. Then the cursor is incremented.

### READ

The page memory location addressed by the cursor is written into the mail box.

Then the cursor is incremented.

These two modes give sequential access to the page memory.

### WRITE, READ WITHOUT INCREMENTATION

Same as above but the cursor is not incremented.

### WRITE SLICE

This mode is used to load a RAM used as extended character generator.

The execution takes two cycles :

- A read without incrementation cycle is performed on the page memory. The character code is latched in the extended character code register. A7, B(5:7) are latched in VIN.
- The contents of the TA register of the mail box is written into the character generator. The address is given by the extended character code register and the contents of NT, which is sent on ADR(0:3). The extension condition B7 ∧ (B5 ∨ B6) is sent on ADR4. Then NT is incremented modulo 10.

### READ SLICE

This mode is used to read a slice in any character generator.

The execution takes 2 cycles :

- The first cycle is identical to the first cycle of WRITE SLICE.
- On the second cycle, a character 8-bit slice is written into the mail box.

NOTA :

1. In READ or WRITE SLICE mode, the character code address is indirectly given by the cursor. The page memory must have been previously initialized.
2. The first data transfer following the loading of any READ mode into the M register is triggered by a mail box read by the microprocessor. Consequently these first data are invalid.
3. Any access of the mail box by the internal bus resets the busy flip flop. If the display is disabled, then the busy flip flop remains set for a maximum of 4 window periods, otherwise a maximum of 44 window periods.

## TIMING GENERATOR AND INTERNAL BUS CYCLES

### LINES AND FRAME

The input clock is at half the dot frequency (3.5 MHz). 8 dot periods (4 clock periods) make a window period. 56 window periods make a line period (≃ 64 µs).

TL output is at line frequency. The duration of TL is programmable through R5 (Display and Timing Generator Mode Register).

With R5 = 0, TL output is at "0" (low level) for 4 window periods (≃ 4.5 µs).

With R5 = 1 (Monitor Mode), TL output is at "1" (high level) for 16 window periods (18.3 µs). In this mode, TL may directly drive the horizontal deflection circuitry. To protect the Darlington from overloading, the TL output is set to "1" when a low level is applied on $\overline{RES}$ and remains in this state until reception of a LOAD R command.



## MICROPROCESSOR INTERFACE

The complete display unit is accessed by the processor through 4 addresses when $\overline{CS}$ is low and E is high.

| ADDRESS | | ADDRESSED REGISTER | | |
|---|---|---|---|---|
| $C/\overline{T}$ | $B/\overline{A}$ | $R/\overline{W} = 1$ Read | $R/\overline{W} = 0$ Write | Comments |
| 0 | 0 | TA | TA | A 16 bit data is read or written from/into the mail box |
| 0 | 1 | TB (1) | TB (1) | |
| 1 | 0 | Busy (2) | TA | A 16 bit command is written in the mail box or the busy flip-flop is read (4). |
| 1 | 1 | – (3) | TB (1) | |

(1) Sets the busy flip-flop and activates $\overline{VE}$.
(2) Busy is read MSB on the MPU bus (D7). Other bits are don't care.
(3) Illegal operation.
(4) A valid command should be loaded at least [illegible] µs after power on or RESET without testing busy to reset it.

### COMMAND – ($C/\overline{T} = 1$)

When the mail box is written with a command, the busy flip flop is set and GEN activates $\overline{VE}$. A Read command request ($\overline{VE}$ low and $C/\overline{T}$ high) is memorized by the access automaton of VIN. As soon as the access automaton takes control over the internal bus, it reads the command in the mail box ; this resets the busy flip-flop. 11 bits only out of the 16 bits of the command are read :

B (5:7) give the address of the register or the operation to perform.

A (0:7) give a parameter.

4 registers may be modified by a command : the Cursor Register C, the Origin Register Y0, the Access Mode Register M and the Display and Timing Mode Register R.

| COMMAND CODE | | | | | | | | | | | | | | | | NAME | OPERATION |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | | |
| 0 | 0 | 0 | | | | | | | | | K (0 : 4) | | | | | Begin Row | X (0 : 5) ⟵ C<br>Y (0 : 4) ⟵ K (0 : 4) |
| 0 | 0 | 1 | | | | | | | | | K (0 : 4) | | | | | Load Y | Y (0 : 4) ⟵ K (0 : 4) |
| 0 | 1 | 0 | | | | | | | | K (0 : 5) | | | | | | Load X | X (0 : 5) ⟵ K (0 : 5) |
| 0 | 1 | 1 | | | | | | | | | | | | | | INC C | C ⟵ C + 1 |
| 1 | 0 | 0 | | | | | | K (0 : 7) | | | | | | | | Load M | M (0 : 7) ⟵ K (0 : 7) |
| 1 | 0 | 1 | | | | | | K (0 : 7) | | | | | | | | Load R | R (0 : 7) ⟵ K (0 : 7) |
| 1 | 1 | 0 | | | | | | | | K (0 : 5) | | | | | | Load Y0 | Y0 (0 : 5) ⟵ K (0 : 5) |
| 1 | 1 | 1 | | | | | | | | | | | | | | | Not interpreted |

The first 4 commands allow cursor handling :

- Initialization at the beginning of a row
- Vertical movement
- Horizontal movement
- Incrementation

## DISPLAY AND TIMING MODE REGISTER R(0:7)

R(0:7) is an 8-bit register.
This register is loaded through a LOAD R command.
The 6 bits R(0:4) and R7 define the display modes.
The 2 bits R(5,6) define the timing modes.

| R0 | R1 | Condition | I | R G B |
|---|---|---|---|---|
| 0 | — | — | 0 | Black |
| 1 | 0 | — | — | — |
| 1 | 1 | In boxing zone | 1 | — |
| 1 | 1 | Outside boxing zone | 0 | Black |

Bit 0 : When R0 = 0, the display automaton is disabled. R, G, B and I outputs stay low. When R0 = 1, the display automaton is enabled. When the display automaton is disabled, loading the R register with R0 = 1 may alter the page memory contents if not done during the vertical blanking intervals.

Bit 1 : When R1 = 0, the boxing attribute is disabled. I stays high, during the display periods. When R1 = 1, the boxing attribute is enabled. R, G, B and I outputs are low out of the boxing zone. I is high in the boxing zone. The CRT and VIN are supposed to be synchronized by a composite external video signal. I switches the boxed windows on the screen.

Bit 2 : When R2 = 0, the conceal attribute is disabled. When R2 = 1, the conceal attribute is enabled.

Bit 3 : When R3 = 1, the service row is displayed at the top of the screen. When R3 = 0, it is concealed.

Bit 4 : When R4 = 1, the cursor position is displayed. The character in the window alternates between normal and reverse video at blinking frequency. When blinking is disabled (R7 = 0), it is permanently reversed. When R4 = 0, the cursor position is not displayed.

Bit 5 : When R5 = 0, TL is active low during 4 window periods. When R5 = 1, TL is active high during 16 window periods.

Bit 6 : When R6 = 0, TT period is 262 lines (60 Hz). When R6 = 1, TT period is 312 lines (≃ 50 Hz).

Bit 7 : When R7 = 0, blinking is disabled. When R7 = 1, blinking is enabled.

## CURSOR REGISTER C

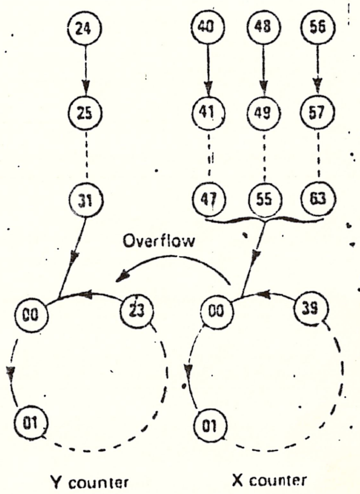
The cursor register C points to the page memory. It is subdivided into two counters X and Y :

X(0:5) points to a column. The decimal value of X comes from 00 to 39 when columns are addressed from left to right.

Y(0:4) points to a row. The decimal address of the service row is 31. The other rows are addressed from 00 to 23.

When the cursor is incremented, X is incremented. When X overflows, Y is automatically incremented as shown in the state diagram below.

Nota : the 11 bits of X and Y are transcoded to get a 10 bit binary address in the page memory.




X5=0 até coluna 31
X5=1 após coluna 31

STATE DIAGRAM

512 256 128 64 32 16 8 4 2 1

| $Y_4 Y_3$ | | ADR9 | ADR8 | ADR7 | ADR6 | ADR5 | ADR4 | ADR3 | ADR2 | ADR1 | ADR0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 00 | X5 = 0 | Y4 | Y3 | Y2 | Y1 | Y0 | X4 | X3 | X2 | X1 | X0 |
| 10 | | | | | | | | | | | |
| 01 | X5 = 1 | 1 | 1 | Y2 | Y1 | Y0 | Y4 | Y3 | X2 | X1 | X0 |
| 11 | — | 1 | 1 | X5 | X4 | X3 | 1 | 1 | X2 | X1 | X0 |

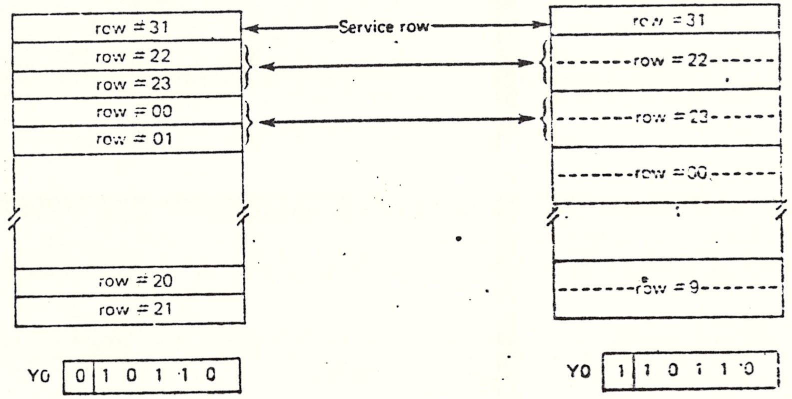


## ORIGIN REGISTER Y0(0:5)

Y0(0:5) is a 6 bit register.
This register is loaded through a LOAD Y0 command.

Bit 0 to 4 : Y0 (0:4) give the number of the first row displayed directly after the service row. A circular roll up or roll down may be commanded by incrementing or decrementing modulo 24 the value of Y0(0:4).

Bit 5 : Y0(5) = 1 sets the zoom mode : the first 12 rows are displayed in double height. If a character was already displayed in double height, it is now in quadruple height. The service row is always displayed in single height. Y0(5) = 0 resets the zoom mode.




No zoom mode
First displayed row = 22

Zoom mode
First displayed row = 22

## ACCESS MODE REGISTER M(0:7)

M(0:7) is an 8 bit register.
This register is loaded through a LOAD M command.
Subsequent data transfers are executed according to the current access mode (see "Data transfer".)

| ACCESS MODE REG. | | | | | | | | ACCESS MODE | SUBSEQUENT DATA TRANSFER |
|---|---|---|---|---|---|---|---|---|---|
| M7 | M6 | M5 | M4 | M3 | M2 | M1 | M0 | | |
| 0 | 0 | 0 | | | | | | Write | MP (C) ← T ; C ← C+1 |
| 0 | 0 | 1 | | | | | | Read | T ← MP (C) ; C ← C+1 |
| 0 | 1 | 0 | | | | | | Write without INC | MP (C) ← T |
| 0 | 1 | 1 | | | | | | Read without INC | T ← MP (C) |
| 1 | 0 | 0 | | | NT | | | Write slice | GC (MP(C), NT) ← T ; NT ← NT+1 |
| 1 | 0 | 1 | | | NT | | | Read slice | T ← GC (MP(C), NT) ; NT ← NT+1 |
| 1 | 1 | | | | | | | Illegal | |

NT : Slice number    T : Mail Box    C : Cursor    MP : Page Memory    GC : Character Generator

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