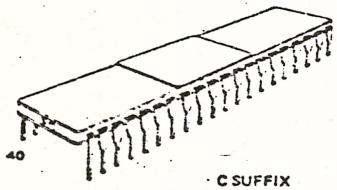
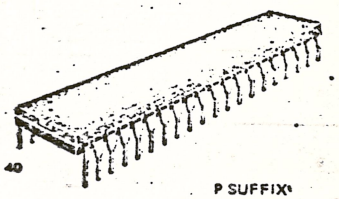
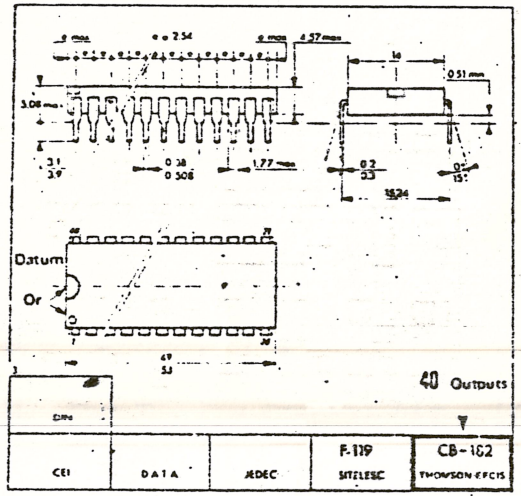
CASE CB-182



C SUFFIX
CERAMIC PACKAGE



P SUFFIX
PLASTIC PACKAGE



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THOMSON-EFCIS

Integrated Circuits

EF9340
EF9341

ADVANCE INFORMATION

MOS

(N CHANNEL, SILICON GATE)

VIDEOTEX CRT DISPLAY PROCESSOR

VIDEOTEX CRT DISPLAY PROCESSOR

Two 40 pin circuits EF9340 (VIN) and EF9341 (GEN) and 16 K bits of standard static RAM are enough to build a complete display unit for an interactive or broadcast videotex terminal :

- Simple, low cost yet flexible, asynchronous interface with microprocessor
- Display of 25 or 21 rows of 40 characters
- On chip (GEN) 128 alphanumeric and 123 semi graphic character generator
- Easy extension up to 2 additional sets of 96 characters each
- One colour, double height, double width, negative (alphanumeric) or two colours (semi-graphic) and blinking are provided as parallel attributes
- Conceal, boxing, underlining as serial attributes
- Programmable roll up, roll down, zoom, and cursor display
- 50 Hz/60 Hz operation
- On chip R, G, B shift registers (VIN)
- Half dot frequency (3.5 MHz) clock input
- Vertical synchronization input
- Single + 5 Volt supply
- TTL/MOS compatible I/O

CASE CB-182

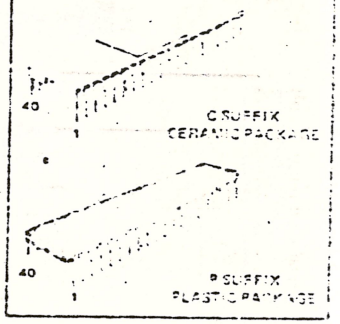
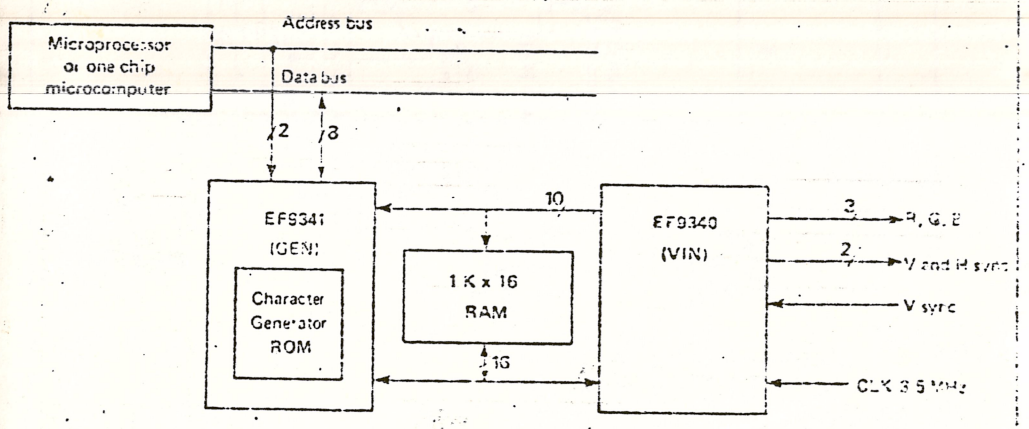


FIGURE 1 – TYPICAL DISPLAY UNIT



Registered patent ANTIOPE PTT/TDF

B7	B6	B5	B4	MOSAIC Semi-graphic	SEPARATED Semi-graphic
0	1	0	0		
0	1	0	1		
0	1	1	0		
0	1	1	1		
1	0	0	0		
1	0	0	1		
1	0	1	0		
1	0	1	1		

B3	B2	B1	B0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

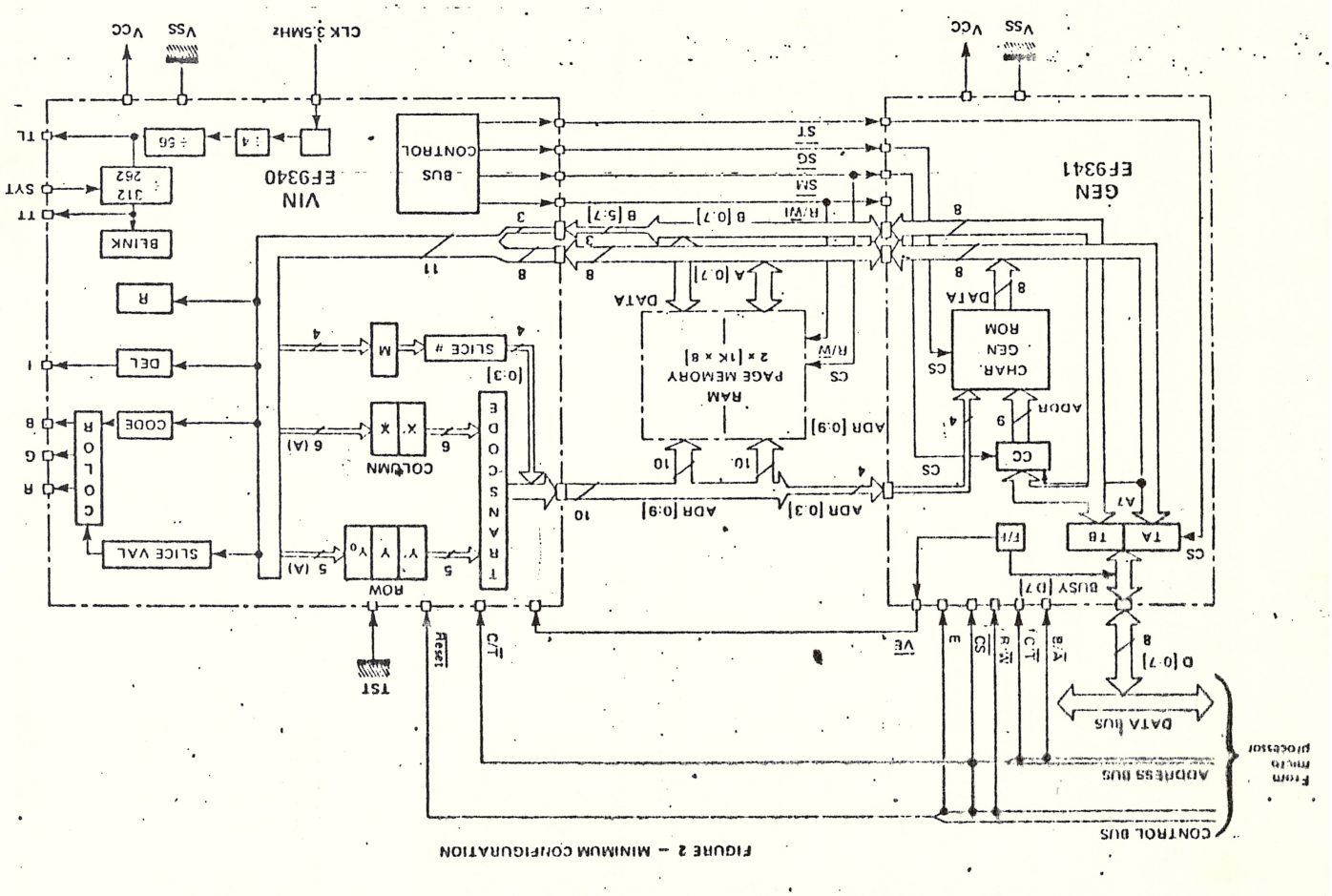
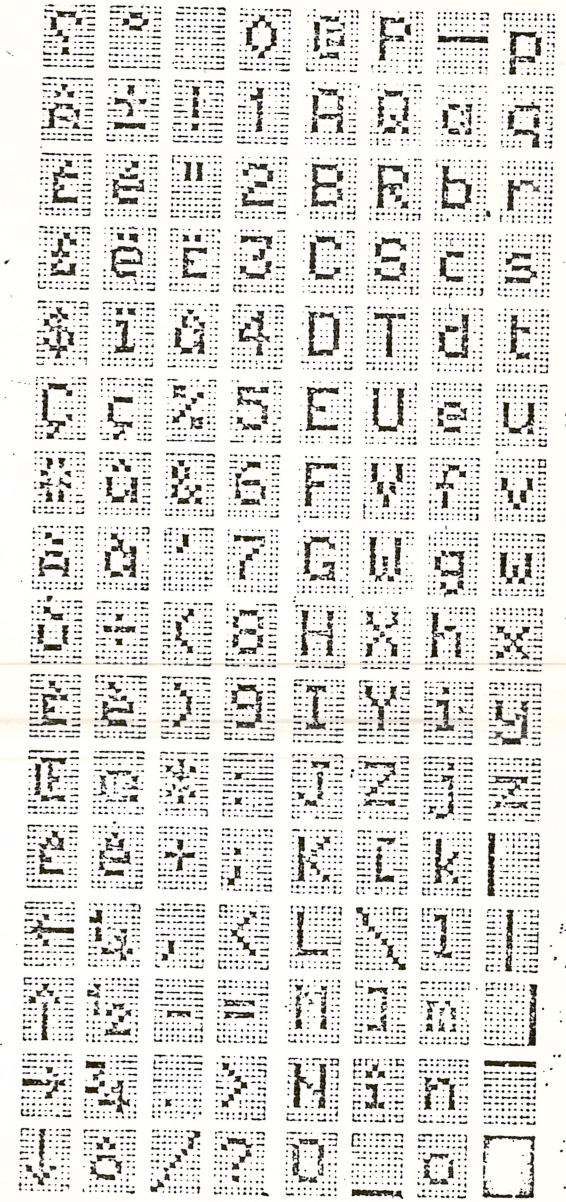


FIGURE 2 – MINIMUM CONFIGURATION

ALPHANUMERIC CHARACTER SET

B7	0	0	0	0	0	0	0	0
B6	0	0	0	0	1	1	1	1
B5	0	0	1	1	0	0	1	1
B4	0	1	0	1	0	1	0	1
B3	B2	B1	B0					
0	0	0	0					
0	0	0	1					
0	0	1	0					
0	0	1	1					
0	1	0	0					
0	1	0	1					
0	1	1	0					
0	1	1	1					
1	0	0	0					
1	0	0	1					
1	0	1	0					
1	0	1	1					
1	1	0	0					
1	1	0	1					
1	1	1	0					
1	1	1	1					



NOTA : Black dots output high (GEN)

GENERAL OPERATION DESCRIPTION

The display unit is organized around a 16 bit internal bus (fig.2) controlled by VIN. GEN contains a character generator and two 8 bit registers – TA and TB – which provide a buffered interface with a general purpose 8 bit bus. The display unit receives data and commands through these registers which perform as a mail box. VIN contains a Timing Generator, a Display Automaton and an Access Automaton.

TIMING GENERATOR

It divides the clock input at half the dot frequency (3.5 MHz) by 4 to get the window frequency. This frequency is divided to get the line frequency and the frame frequency. The size of a character being programmable, it occupies 1, 2 or 4 windows on the screen. Each window is 10 TV lines high and 8 dots wide. Timing Generator gives control over the bus to the display automaton for 40 window periods per line and 250 (or 210) lines per frame. Access automaton has control over the internal bus for the remaining time.

DISPLAY AUTOMATON

During each displayable window period ($\simeq 1.1\ \mu s$), the display automaton controls two read cycles on the internal bus.

On the first cycle, a window code (16 bits) is read from the page memory (table 1). Attribute field (7 bits) and character type field (4 bits) are latched in VIN.
Character code field (9 bits) is latched in CC registers.

Then window address register is incremented.
On the second cycle, address bus gives the slice number (0 – 9) to the character generator and a slice of 8 dots is read. Then Display Automaton delivers G, B signals and I (boxing command).
A set of 128 alphanumeric characters and a set of 64 standard semi-graphic characters are provided by CGR. Further extension is easily done using standard (1k x 8) ROM or RAM components (fig. 8).

ACCESS AUTOMATON

When TA register and then TB register of the mail box are written from the main bus with $C/\overline{T} = 1$, Access Automaton knows that a command is pending.
As soon as it gets control over the internal bus, it reads the mail box and gets the command.
A command may be :

- A cursor modification
- A display mode (ON, OFF, Roll up, etc...)
- A data transfer mode (Read/Write Page Memory, Read/Write Character Generator)

Data transfers are executed through the mail box addressed with $C/\overline{T} = 0$ and according to the current Data Transfer Mode.

The busy flip-flop gives the status of the mail box. It can be read in the MSB of the TA byte addressed with $C/\overline{T} = 1$.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC} *	−0.3 to + 7.0	Vdc
Input Voltage	V_{in} *	−0.3 to 7 V	Vdc
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	−55 to + 150	°C
Max Power Dissipation	P_{DM}	0.75	W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

* With respect to V_{SS}

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ± 5 %, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Supply Voltage		V_{CC}	4.75	5.0	5.25	Vdc
Input Low Voltage		V_{IL}	−0.3	–	0.8	Vdc
Input High Voltage (except SYT and CLK)		V_{IH}	2.2	–	V_{CC}	Vdc
Input High Voltage SYT and CLK		V_{IH}	3	–	V_{CC}	Vdc
Three State and Input Leakage current (except CLK)		I_{in}	–	–	10	µA
CLK input current	V_{IN} = 0.4 V	I_{IL}	–	–	− 2	mA
Output High Voltage I_{load} = −150 µA I_{load} = −500 µA	R, G, B, I Other outputs	V_{OH}	2.4	–	–	V
Output Low Voltage I_{load} = 0.4 mA I_{load} = 1.6 mA	R, G, B, I Other outputs	V_{OL}	–	–	0.4	V
Power Dissipation VIN GEN		P_D	–	200 250	–	mW
Input Capacitance		C_{in}	–	–	10	pF

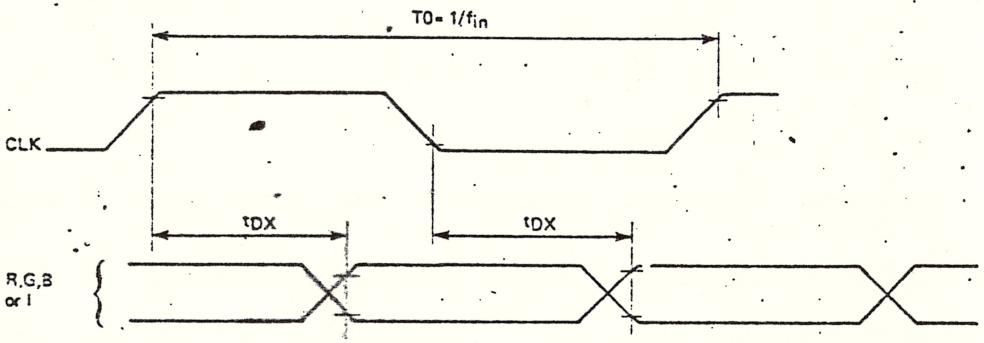


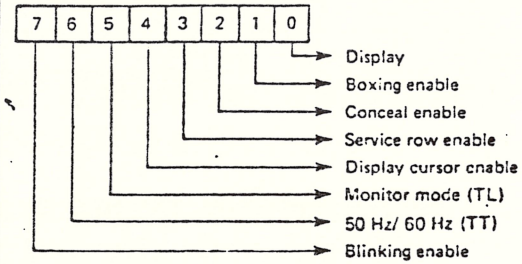
FIGURE 3 – R, G, B and I TIMING (VIN)

CLOCK R, G, B AND I TIMING CHARACTERISTICS (V_{CC} = 5.0 ± 5 %, V_{SS} 0, T_A = 0 – 70° C, CL = 70 pF)

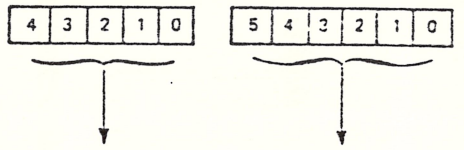
Characteristic	Symbol	Min	Typ	Max	Unit
Clock frequency	f_{in}	3.4	–	3.6	MHz
R, G, B or I delay time from clock edge	tDX	–	–	130	ns
R, G, B and I relative delay		–	5	–	ns

REGISTERS

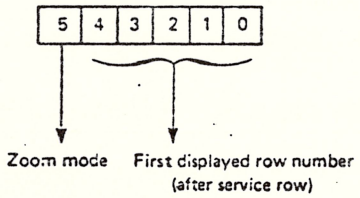
DISPLAY AND TIMING MODE REGISTER R



CURSOR REGISTER C



ORIGIN REGISTER Y0



ACCESS MODE REGISTER M

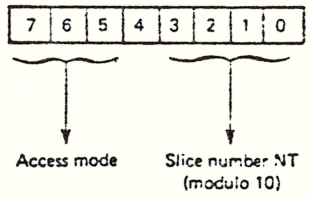


TABLE 2 — COMMAND CODE

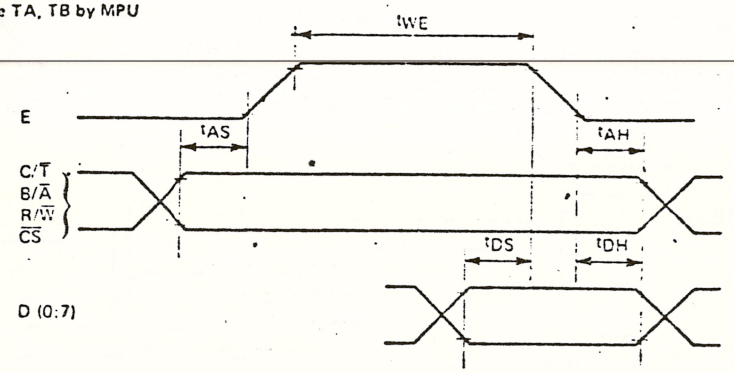
COMMAND CODE																NAME	OPERATION
B7	B6	B5	B4	B3	B2	B1	B0	A7	A6	A5	A4	A3	A2	A1	A0		
0	0	0									K (0 : 4)					Begin Row	X (0 : 5) ⟵ 0 Y (0 : 4) ⟵ K (0 : 4)
0	0	1									K (0 : 4)					Load Y	Y (0 : 4) ⟵ K (0 : 4)
0	1	0									K (0 : 5)					Load X	X (0 : 5) ⟵ K (0 : 5)
0	1	1														INC C	C ⟵ C + 1
1	0	0						K (0 : 7)								Load M	M (0 : 7) ⟵ K (0 : 7)
1	0	1						K (0 : 7)								Load R	R (0 : 7) ⟵ K (0 : 7)
1	1	0									K (0 : 5)					Load Y0	Y0 (0 : 5) ⟵ K (0 : 5)
1	1	1															Not interpreted

TABLE 3 — ACCESS MODE REGISTER

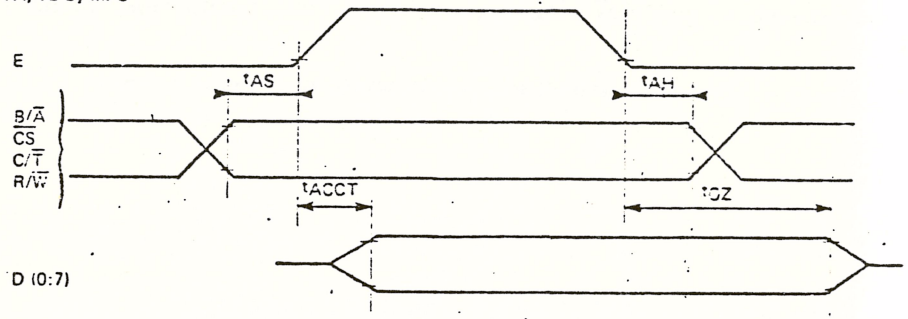
ACCESS MODE REG.								ACCESS MODE	SUBSEQUENT DATA TRANSFER
M7	M6	M5	M4	M3	M2	M1	M0		
0	0	0						Write	MP (C) ⟵ T ; C ⟵ C + 1
0	0	1						Read	T ⟵ MP (C) ; C ⟵ C + 1
0	1	0						Write without INC	MP (C) ⟵ T
0	1	1						Read without INC	T ⟵ MP (C)
1	0	0			N	T		Write slice	GC (MP(C), NT) ⟵ T ; NT ⟵ NT + 1
1	0	1			N	T		Read slice	T ⟵ GC (MP(C), NT) ; NT ⟵ NT + 1
1	1							Illegal	

NT : Slice number T : Mail Box C : Cursor MP : Page Memory GC : Character Generator

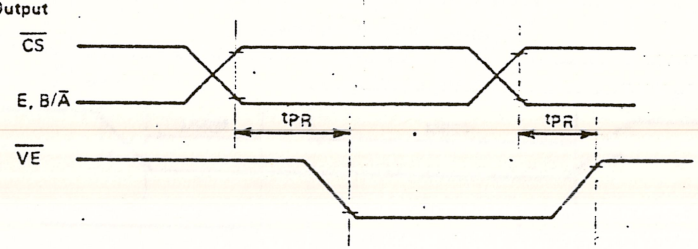
Write TA, TB by MPU



Read TA, TB by MPU



VE Output



Reference level : Input 0.8 and 2.2 V
Output 0.4 and 2.4 V

FIGURE 4 — PROCESSOR BUS TIMING CHART (GEN)

PROCESSOR BUS TIMING CHARACTERISTICS
(V_{CC} = 5.0 V ± 5 %, V_{SS} = 0, T_A = 0 to 70° C — C_L = 100 pF on all outputs

Characteristic	Symbol	Min	Typ	Max	Unit
Enable pulse duration	tWE	200	—	—	ns
Address setup time	tAS	40	—	—	ns
Address hold time	tAH	0	—	—	ns
Data setup time	tDS	140	—	—	ns
Data hold time	tDH	10	—	—	ns
TA, TB access time	tACCT	—	—	220	ns
Data off time	tOZ	0	—	220	ns
VE delay time (CS = 0 ; E = B/A = 1)	tPR	—	—	140	ns

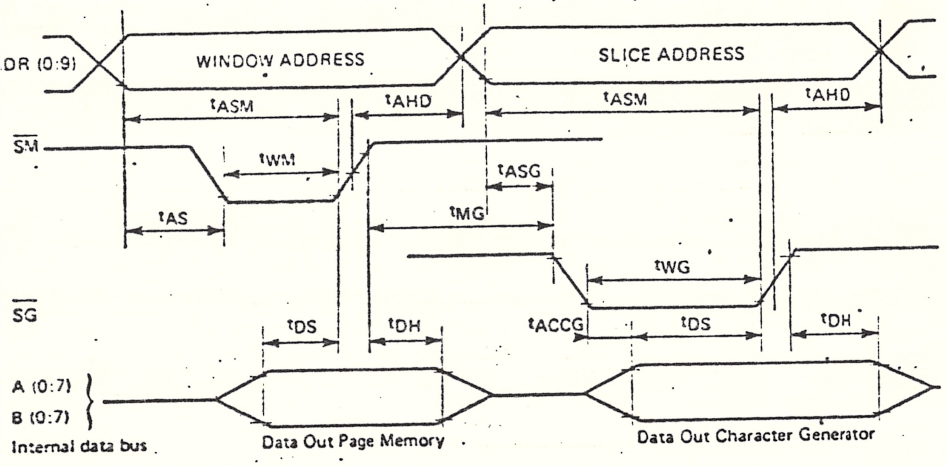


FIGURE 5 – INTERNAL BUS - DISPLAY READ CYCLES – TIMING CHART (R/$\overline{W}$i = 1)

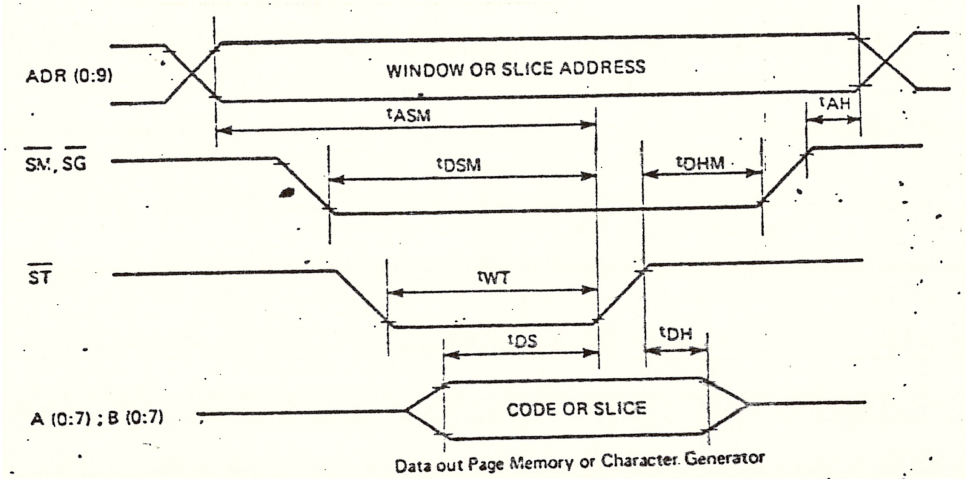


FIGURE 6 – INTERNAL BUS – FROM PAGE MEMORY OR CHARACTER GENERATOR TO MAIL BOX TRANSFER CYCLES (R/$\overline{W}$i = 1)

TABLE 1 – CHARACTER CODES

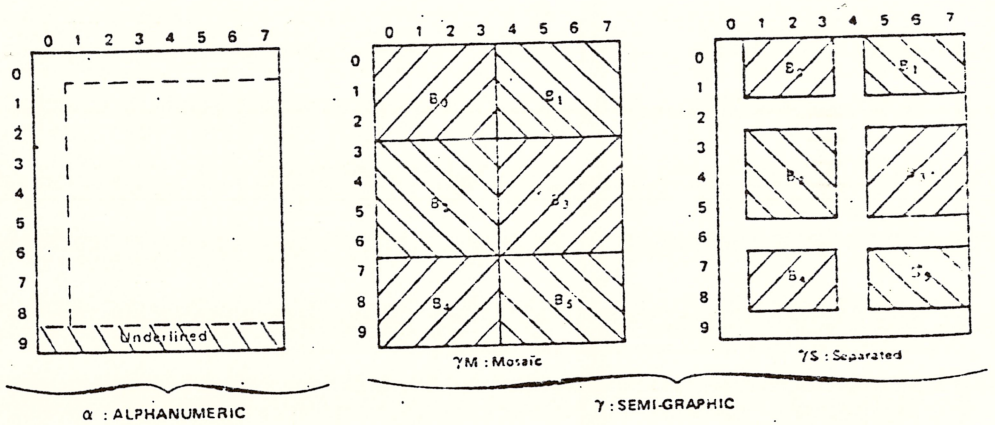
WINDOW CODE IN PAGE MEMORY																COMMENTS			
Type and character code field									Attribute field							Type	Implicite Attribute	Ad-hoc Serial Attribute	Remark
B7	B6	B5	B4	B3	B2	B1	B0	A7	A6	A5	A4	A3	A2	A1	A0				
0	X	X	X	X	X	X	X	0	N	L	H	S	B_1	G_1	R_1	α_0 (128)		Undefined C_0	in CEN
1	0	0	—	—	s	i	m	0	B_0	G_0	R_0	—	B_1	G_1	R_1	DEL			
1 1 1	0 1 1	1 0 1	X	X	X	X	X	0	N	L	H	S	B_1	G_1	R_1	α_1 (56)		C_0	EXTENSION
0	0	X	X	X	X	X	X	1	B_0	G_0	R_0	S	B_1	G_1	R_1	γS (54)	Normal size, positive		in CEN
0	1	X	X	X	X	X	X	1	B_0	G_0	R_0	S	B_1	G_1	R_1	γM (64)			
1	0	0	—	—	—	—	—	1	—	—	—	—	—	—	—	ILLEGAL			
1 1 1	0 1 1	1 0 1	X	X	X	X	X	1	B_0	G_0	R_0	S	B_1	G_1	R_1	γ_1 (96)	Normal size		EXTENSION

Note : Extension for α 1 and γ 1 may be mapped in only one 1 K x 8 RAM or ROM.

GLOSSARY :

α	:	Alphanumeric
γ	:	Semi-graphic
γS	:	Separated semi-graphic
γM	:	Mosaic semi-graphic
DEL	:	Delimitor
m	:	Blanking
i	:	Boxing
s	:	Underlining

C_0 (R_0, G_0, B_0)	:	Background colour
C_1 (R_1, G_1, B_1)	:	Foreground colour
H	:	Double height
L	:	Double width
N	:	Reverse video (negative)
S	:	Stable (non blinking)
X	:	Character code
—	:	Don't care



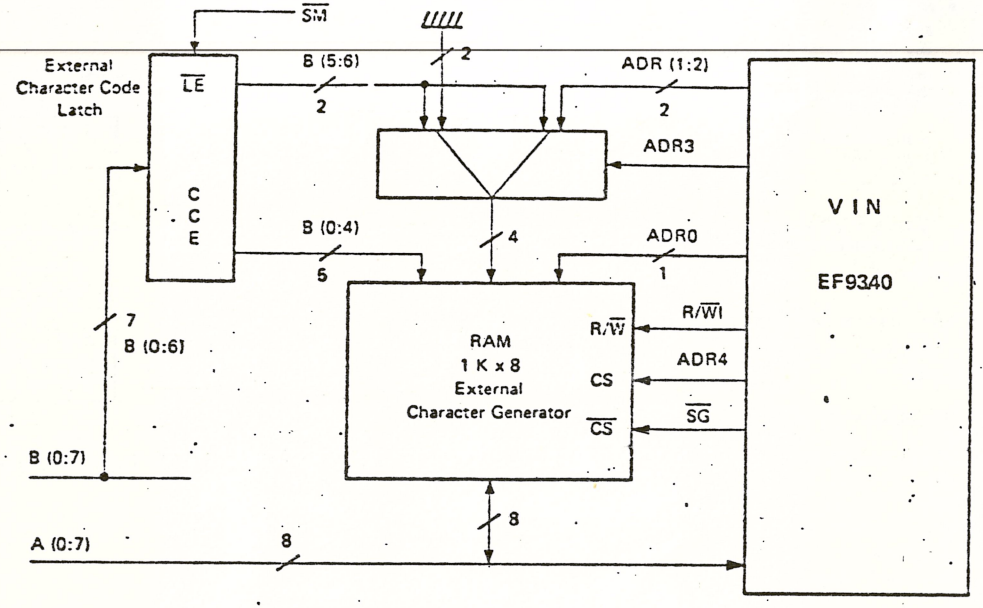


FIGURE 8 – ADDING AN EXTERNAL CHARACTER GENERATOR

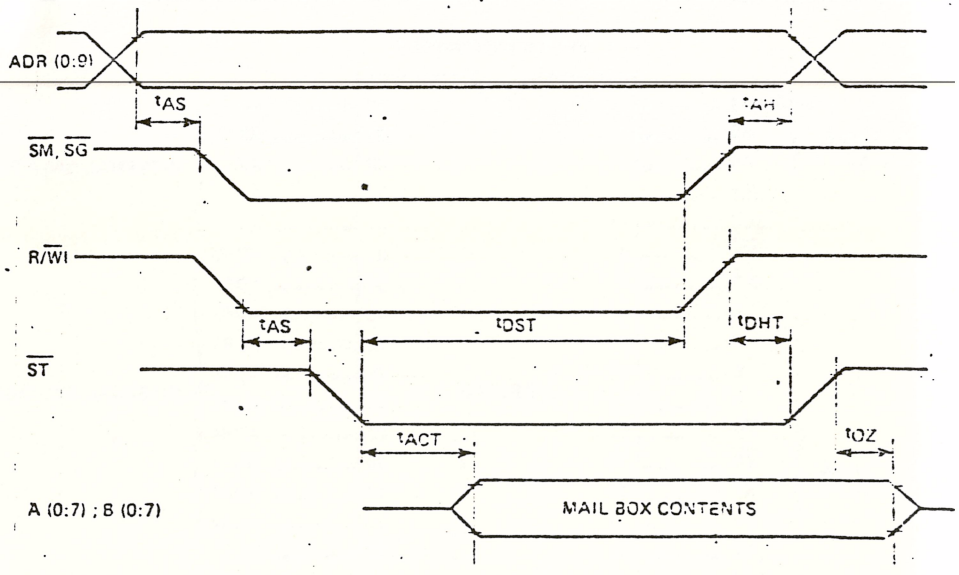


FIGURE 7 – INTERNAL BUS – FROM MAIL BOX TO PAGE MEMORY OR CHARACTER GENERATOR OR VIN TRANSFER CYCLES

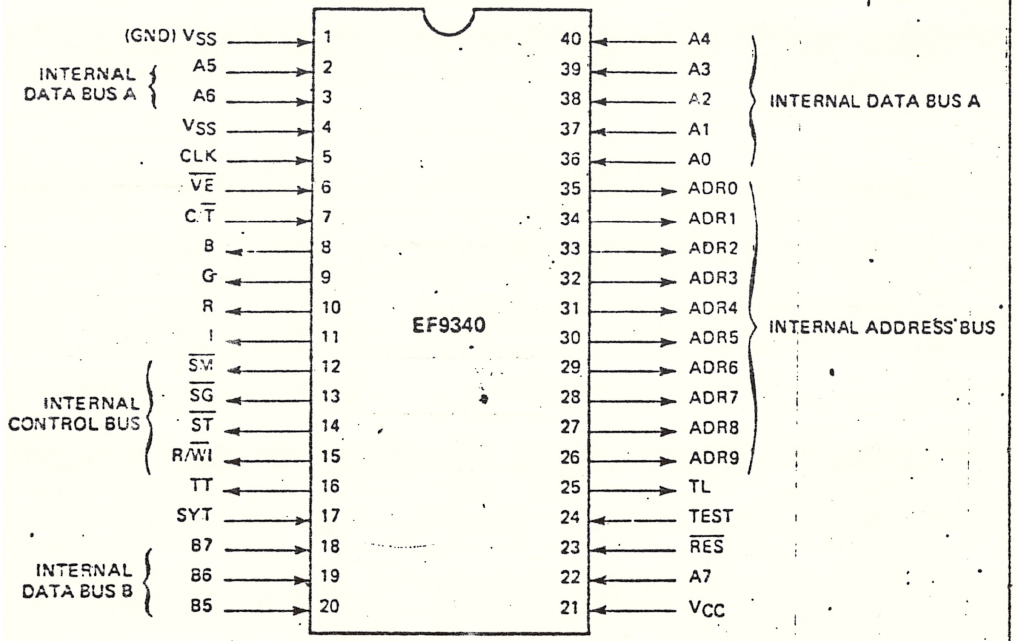
INTERNAL BUS TIMING CHARACTERISTICS

(V_{CC} = 5.0 V ± 5 %, V_{SS} = 0, T_A = 0 to 70° C, C_L = 100 pF on all outputs, f_{in} = 3.5 MHz)

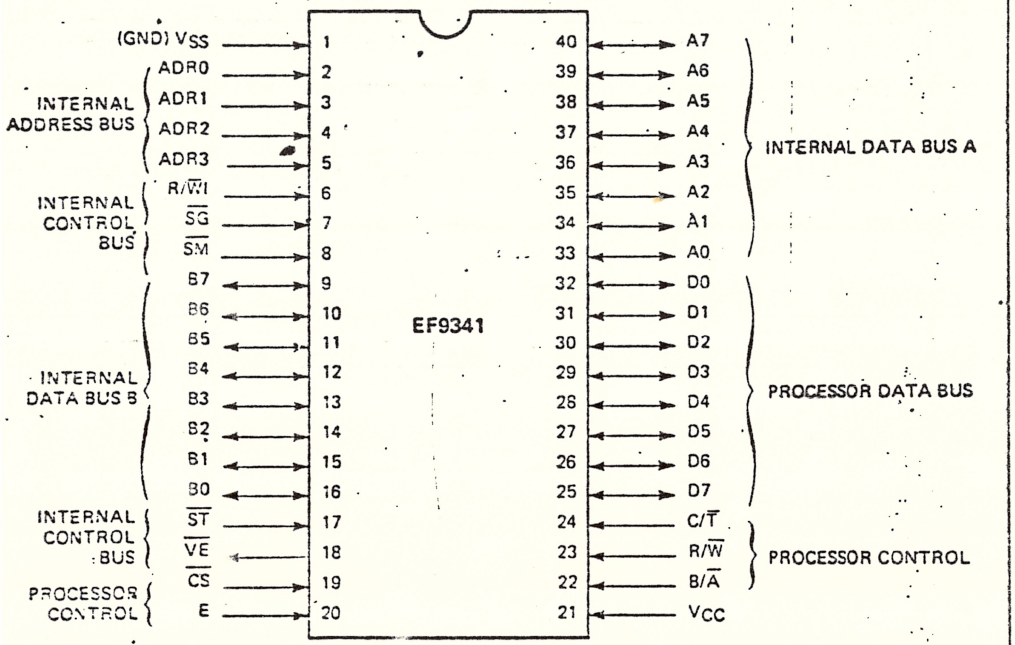
Characteristic	Symbol	Min	Typ	Max	Unit
Address setup time	tASM	450	–	–	ns
Address hold time	tAH	0	–	–	ns
Strobe duration (display cycles)	tWM	300	–	–	ns
	tWG	280	–	–	ns
Address hold time (display cycles) (Ref. 1.5 V for SM, SG, ADR)	tAHD	0	0	–	ns
Address to strobe	tASG	40	–	–	ns
Data setup time	tDS	140	–	–	ns
Data hold time	tDH	0	–	–	ns
Precharge Character Generator (in GEN)	tMG	60	–	–	ns
Access to Character Generator (in GEN)	tACCG	–	–	240	ns
From SM or SG to ST	tDSM	400	–	–	ns
SM or SG hold time	tDHM	0	–	–	ns
Write Mail Box strobe duration	tWT	250	–	–	ns
Write setup time	tAS	40	–	–	ns
From ST to SM or SG	tDST	300	–	–	ns
Access time to Mail Box (in GEN)	tACT	–	–	220	ns
ST hold time	tDHT	60	–	–	ns
Mail Box off time	tOZ	0	–	270	ns

Reference level : 0.8 V and 2 V on any input
0.4 V and 2.4 V on any output } unless otherwise specified.

VIN PIN ASSIGNMENT



GEN PIN ASSIGNMENT



- double height : the slices of the pattern are repeated so as to get a 20 x 8 double pattern. If the row is H even, the upper pattern is kept, otherwise lower pattern is kept.
  The double pattern is obtained by :

  – tripling slice 0
  – doubling slice 1 to 8
  – keeping slice 9

  Double height and double width may be combined to get a double size.

Colors

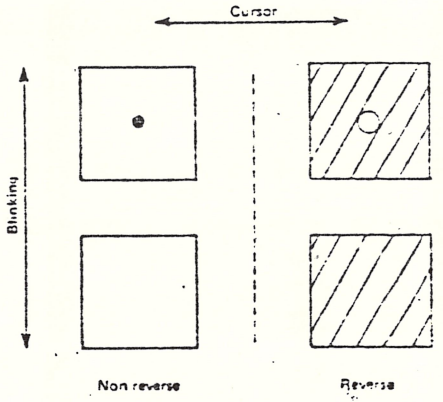
Each bit of the final 10 x 8 pattern corresponds to a pixel.

The color of the pixel is C_0 if the bit value is 0. Otherwise, it is C_1.

Boxing, conceal

If the conceal is enabled (R2 = 1), and if the window is in a conceal zone, then the colors in the window are reset to black.

If the boxing is enabled (R1 = 1), and if the window is out of a boxing zone, the color resets to black in the window and I output is low. The window is "transparent".



Non Reverse and reverse character display with blinking or in cursor position.

DISPLAY OF DELIMITORS

In the 10 x 8 implicit pattern associated with a delimitor, all the bits have the same value : 1.

"cursor" position : the pattern is periodically reset.

colors : same as any other type : a delimitor is displayed as a space in color C_1.

boxing : if the boxing is enabled (R5 = 1), and if the delimitor defines a boxing zone border, half of the window is transparent. Out of boxing zone, a delimitor is completely transparent.

Remark : the value of the lining and the conceal bits given by a delimitor is ignored in the window associated with this delimitor.

CHARACTER GENERATORS

GEN contains a CC register ; a standard 128 character α_0 set and a standard 128 semi graphic γ set.

Further extension of these character sets is easily done by adding 1 K x 8 standard ROM or RAM components (fig 8).

A latch CCE is loaded by the character code with $\overline{SM}$.

A quad 2 to 1 multiplexer transcodes 11 bits of logical address. — 96 character codes CCE (0 : 6) by 10 slice address codes ADR(0:3) — to 10 bits of physical address.

Logical Address

ADR3 = 0	CCE6	CCE5	CCE4	CCE3	CCE2	CCE1	CCE0	ADR2	ADR1	ADR0
ADR3 = 1	0	0	CCE4	CCE3	CCE2	CCE1	CCE0	CCE6	CCE5	ADR0

The external character generator is selected by ADR4 high and $\overline{SG}$ low. It is read or written whether R/$\overline{W}$ is high or low.

CHARACTER ATTRIBUTES

SERIAL ATTRIBUTES, PARALLEL ATTRIBUTES

The shape to be displayed in a window is defined by :
- a pattern held in the character generators and addressed by the CC field of the window code.
- the actual value of the attributes.

The attributes are :
- C_f (3 bits) and C_t (3 bits) : 2 colours
- Blinking (1)
- Double height (1) , Double width (1)
- Reverse video (1)
- Boxing (1)
- Conceal (1)
- Underlining (1)

In any column 0 window, their implicit value is C_0 = black, not boxed, not concealed, not underlined. The window code defines the type of the character to be displayed in this window and the value of its parallel attributes (see table 1). The value of the remaining attributes is serially defined by scanning the windows from left to right (column 0 to 39) then up to down. Therefore, any other type of character gives the values of C_0 for a subsequent string of alphanumerics. Besides, a delimitor gives the value of the boxing, conceal and underlining attributes for the following windows. A boxing zone is a string of windows belonging to the same row, in which the boxing attribute value is 1.

DOUBLE HEIGHT, DOUBLE WIDTH

- A correct operation assumes that the same window code had been repeated in the page memory (twice for double height or double width, four times for double size).

- No double height windows are supposed to be held in service row.

- No double width character should begin in column 39.

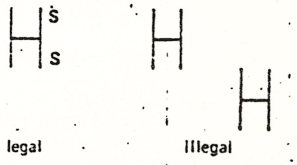
- Single sized, double width, double height and double sized characters may be mixed on a given row.

- But couple of rows bearing double height character should not be interleaved :

More precisely, this attribute defines a H parity for each row :

- service row is H even
- any row is H even if the preceding row does not hold any double height window.
- any row has an H parity reverse to the preceding row if the latter holds at least one double height window.

In the same way, double width define a W parity for the windows as double height for the rows.



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DISPLAY OF NON DELIMITOR TYPES OF CHARACTERS

The display automaton interprets the attributes in the following order :

Underlining

- type α : slice 9 is set in the pattern.

Blinking

- blinking : the pattern is periodically (0.5 Hz) reset. If the video is reversed (α type only), the phase of the blinking clock is complemented. In "cursor" position, the reset does not occur.

Reverse video — Cursor position

- reverse video : (α only). The pattern is complemented.
- cursor position : (any type). The pattern is periodically complemented. If blinking is disabled (R7 = 0), the pattern is permanently complemented.

Double height, double width (α only)

- double width : each bit of the pattern is horizontally doubled so as to get a 10 x 16 double pattern. If the window is W even, only the left pattern is kept. The right pattern is kept if the window is W odd.

VIN SIGNAL DESCRIPTION

VIN controls several types of data transfers on the internal bus.
- From the mail box to VIN
- From the Page Memory to VIN
- From the Character Generator to VIN
- Between Mail Box and Page Memory
- Between Mail Box and Character Generator

VIN delivers R, G, B and synchronization signals to the CRT.

INTERNAL BUS INTERFACE

NAME	PIN TYPE	N°	FUNCTION	DESCRIPTION
A(0:7)	I	36, 37 38, 39 40, 2 3, 22	Internal data bus	VIN gets only eleven inputs out of the sixteen lines of the bidirectional internal data bus.
B(5:7)	I	20-18		
ADR(0:9)	O	35-26	Internal address bus	These ten TTL compatible outputs multiplex the page memory address with the slice number — ADR(0:3) — and the selection of an external character generator — ADR4.
R/$\overline{W}$I	O	15	Read/Write on Internal Bus	This TTL compatible output determines whether the page memory or the character generator gets read or written. A write is active low ("0").
$\overline{SM}$	O	12	Memory strobe	This TTL compatible output, when active, selects the page memory as source (R/$\overline{W}$I high) or destination (R/$\overline{W}$I low) on the internal bus. When $\overline{SM}$ goes active (low), ADR(0:9) and R/$\overline{W}$I are stable.
$\overline{SG}$	O	13	Character generator strobe	This TTL compatible output, when active, selects a character generator as source (R/$\overline{W}$I high) or destination (R/$\overline{W}$I low) on the internal bus. When $\overline{SG}$ goes active (low), ADR(0:4) and R/$\overline{W}$I are stable. $\overline{SM}$ and $\overline{SG}$ are never active at the same time.
$\overline{ST}$	O	14	Mail box strobe	This TTL compatible output, when active, selects the mail box as source (R/$\overline{W}$I low) or destination (R/$\overline{W}$I high) on the internal bus. $\overline{ST}$ may be active (low) at the same time as $\overline{SM}$ or $\overline{SG}$.