CD4066BM/CD4066BC

National Semiconductor

CD4066BM/CD4066BC Quad Bilateral Switch

General Description

The CD4066BM/CD4066BC is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with CD4016BM/CD4016BC, but has a much lower "ON" resistance, and "ON" resistance is relatively constant over the input-signal range.

Features

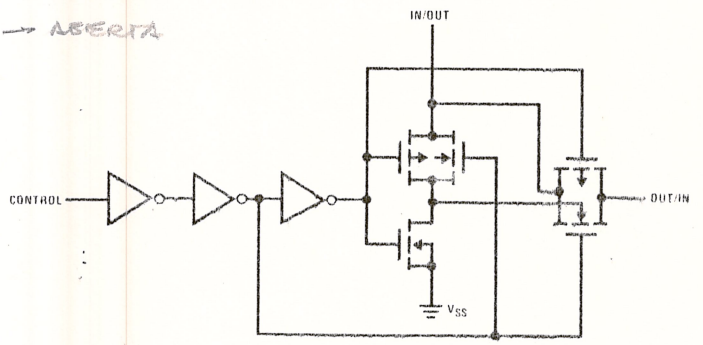
- Wide supply voltage range — 3 V to 15 V
- High noise immunity — 0.45 V_{DD} (typ.)
- Wide range of digital and analog switching — ±7.5 V_{PEAK}
- "ON" resistance for 15 V operation — 80 Ω
- Matched "ON" resistance over 15 V signal input — ΔR_{ON} = 5 Ω (typ.)
- "ON" resistance flat over peak-to-peak signal range
- High "ON"/"OFF" output voltage ratio — 65 dB (typ.) @ f_{is} = 10 kHz, R_L = 10 kΩ
- High degree linearity — 0.1% distortion (typ.) @ f_{is} = 1 kHz, V_{is} = 5 V_{p-p}, $V_{DD} - V_{SS}$ = 10 V, R_L = 10 kΩ
- Extremely low "OFF" switch leakage — 0.1 nA (typ) @ $V_{DD} - V_{SS}$ = 10 V, T_A = 25°C
- Extremely high control input impedance — 10^{12} Ω (typ)
- Low crosstalk between switches — −50 dB (typ) @ f_{is} = 0.9 MHz, R_L = 1 kΩ
- Frequency response, switch "ON" — 40 MHz (typ)

Applications

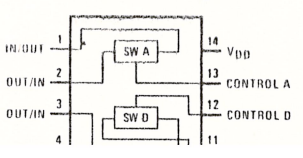
- Analog signal switching/multiplexing
  - Signal gating
  - Squelch control
  - Chopper
  - Modulator/Demodulator
  - Commutating switch
- Digital signal switching/multiplexing
- CMOS logic implementation
- Analog-to-digital/digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal-gain

Schematic and Connection Diagrams

VC = "1" → CERRADA
VC = "0" → ABIERTA



Dual-In-Line Package



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Parameter

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"ON" Resistance

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Input or Output Leaka Switch "OFF"

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Low Level Input Volta

High Level Input Volt

Input Current

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1 and 2)

ply Voltage	−0.5V to +18V
oltage	−0.5V to V_{DD} + 0.5V
Temperature Range	−65°C to +150°C
ssipation	500 mW
Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} Supply Voltage	3V to 15V
V_{IN} Input Voltage	0V to V_{DD}
T_A Operating Temperature Range	
CD4066BM	−55°C to +125°C
CD4066BC	−40°C to +85°C

Electrical Characteristics CD4066BM (Note 2)

Parameter	Conditions	−55°C		25°C			125°C		Units
		Min	Max	Min	Typ	Max	Min	Max	
Quiescent Device Current	V_{DD} = 5V		0.25		0.01	0.25		7.5	μA
	V_{DD} = 10V		0.5		0.01	0.5		15	μA
	V_{DD} = 15V		1.0		0.01	1.0		30	μA
puts and Outputs									
"ON" Resistance	R_L = 10 kΩ to $\frac{V_{DD}-V_{SS}}{2}$								
	V_C = V_{DD}, V_{IS} = V_{SS} to V_{DD}								
	V_{DD} = 5V		2000		270	2500		3500	Ω
	V_{DD} = 10V		400		120	500		550	Ω
	V_{DD} = 15V		220		80	280		320	Ω
"ON" Resistance	R_L = 10 kΩ to $\frac{V_{DD}-V_{SS}}{2}$								
Between any 2 of	V_C = V_{DD}, V_{IS} = V_{SS} to V_{DD}								
4 Switches	V_{DD} = 10V				10				Ω
	V_{DD} = 15V				5				Ω
Input or Output Leakage	V_C = 0		±50		±0.1	±50		±500	nA
Switch "OFF"	V_{IS} = 15V and 0V,								
	V_{OS} = 0V and 15V								
Inputs									
Low Level Input Voltage	V_{IS} = V_{SS} and V_{DD}								
	V_{OS} = V_{DD} and V_{SS}								
	I_{IS} = ±10μA								
	V_{DD} = 5V		1.5		2.25	1.5		1.5	V
	V_{DD} = 10V		3.0		4.5	3.0		3.0	V
	V_{DD} = 15V		4.0		6.75	4.0		4.0	V
High Level Input Voltage	V_{DD} = 5V	3.5		3.5	2.75		3.5		V
	V_{DD} = 10V (see note 6)	7.0		7.0	5.5		7.0		V
	V_{DD} = 15V	11.0		11.0	8.25		11.0		V
Current	V_{DD} − V_{SS} = 15V		±0.1		$\pm 10^{-5}$	±0.1		±1.0	μA
	$V_{DD} \geq V_{IS} \geq V_{SS}$								
	$V_{DD} \geq V_C \geq V_{SS}$								

Electrical Characteristics CD4066BC (Note 2)

DC Electrical Characteristics (Cont'd.) CD4066BC (Note 2)

Parameter		Conditions	−40°C		25°C			85°C	
			Min	Max	Min	Typ	Max	Min	Max
Signal Inputs and Outputs									
R_{ON}	"ON" Resistance	R_L = 10 kΩ to $\frac{V_{DD} - V_{SS}}{2}$ V_C = V_{DD}, V_{SS} to V_{DD}							
		V_{DD} = 5 V		2000		270	2500		3200
		V_{DD} = 10 V		450		120	500		520
		V_{DD} = 15 V		250		80	280		300
ΔR_{ON}	Δ"ON" Resistance Between Any 2 of 4 Switches	R_L = 10 kΩ to $\frac{V_{DD} - V_{SS}}{2}$ V_{CC} = V_{DD}, V_{IS} = V_{SS} to V_{DD}							
		V_{DD} = 10 V				10			
		V_{DD} = 15 V				5			
I_{IS}	Input or Output Leakage Switch "OFF"	V_C = 0		±50		±0.1	±50		±200
Control Inputs									
V_{ILC}	Low Level Input Voltage	V_{IS} = V_{SS} and V_{DD} V_{OS} = V_{DD} and V_{SS} I_{IS} = ±10 μA							
		V_{DD} = 5 V		1.5		2.25	1.5		1.5
		V_{DD} = 10 V		3.0		4.5	3.0		3.0
		V_{DD} = 15 V		4.0		6.75	4.0		4.0
V_{IHC}	High Level Input Voltage	V_{DD} = 5 V	3.5		3.5	2.75		3.5	
		V_{DD} = 10 V (See note 6)	7.0		7.0	5.5		7.0	
		V_{DD} = 15 V	11.0		11.0	8.25		11.0	
I_{IN}	Input Current	V_{DD} − V_{SS} = 15 V $V_{DD} \geq V_{IS} \geq V_{SS}$ $V_{DD} \geq V_C \geq V_{SS}$		±0.3		±10^{-5}	±0.3		±1.0

AC Electrical Characteristics T_A = 25°C, t_r = t_f = 20 ns and V_{SS} = 0 V unless otherwise specified

Parameter		Conditions	Min	Typ	Max
t_{PHL}, t_{PLH}	Propagation Delay Time Signal Input to Signal Output	V_C = V_{DD}, C_L = 50 pF, *(Figure 1)* R_L = 200k			
		V_{DD} = 5 V		25	55
		V_{DD} = 10 V		15	35
		V_{DD} = 15 V		10	25
t_{PZH}, t_{PZL}	Propagation Delay Time Control Input to Signal Output High Impedance to Logical Level	R_L = 1.0 kΩ, C_L = 50 pF, *(Figures 2 and 3)*			
		V_{DD} = 5 V			125
		V_{DD} = 10 V			60
		V_{DD} = 15 V			50
t_{PHZ}, t_{PLZ}	Propagation Delay Time Control Input to Signal Output Logical Level to High Impedance	R_L = 1.0 kΩ, C_L = 50 pF, *(Figures 2 and 3)*			
		V_{DD} = 5 V			125
		V_{DD} = 10 V			60
		V_{DD} = 15 V			50
	Sine Wave Distortion	V_C = V_{DD} = 5 V, V_{SS} = −5 V R_L = 10 kΩ, V_{IS} = 5 V_{p-p}, f = 1 kHz, *(Figure 4)*		0.1	
	Frequency Response–Switch "ON" (Frequency at −3 dB)	V_C = V_{DD} = 5 V, V_{SS} = −5 V, R_L = 1 kΩ, V_{IS} = 5 V_{p-p}, 20 Log_{10} V_{OS}/V_{OS}(1 kHz)−dB, *(Figure 4)*		40	

Electrical Characteristics (Continued)

$T_A = 25°C$, $t_r = t_f = 20$ ns and $V_{SS} = 0$ V unless otherwise noted

Parameter	Conditions	Min.	Typ.	Max.	Units
Feedthrough — Switch "OFF" (Frequency at −50 dB)	$V_{DD} = 5.0$ V, $V_{CC} = V_{SS} = -5.0$ V, $R_L = 1$ kΩ, $V_{IS} = 5.0\ V_{p-p}$, 20 Log_{10}, $V_{OS}/V_{IS} = -50$ dB, *(Figure 4)*		1.25		
Crosstalk Between Any Two Switches (Frequency at −50 dB)	$V_{DD} = V_{C(A)} = 5.0$ V; $V_{SS} = V_{C(B)} = -5.0$ V, $R_L = 1$ kΩ, $V_{IS(A)} = 5.0\ V_{p-p}$, 20 Log_{10}, $V_{OS(B)}/V_{IS(A)} = -50$ dB, *(Figure 5)*		0.9		MHz
Crosstalk; Control Input to Signal Output	$V_{DD} = 10$ V, $R_L = 10$ kΩ, $R_{IN} = 1.0$ kΩ, $V_{CC} = 10$ V Square Wave, $C_L = 50$ pF *(Figure 6)*		150		mV_{p-p}
Maximum Control Input	$R_L = 1.0$ kΩ, $C_L = 50$ pF, *(Figure 7)* $V_{OS(f)} = ½V_{OS}$(1.0 kHz)				
	$V_{DD} = 5.0$ V		6.0		MHz
	$V_{DD} = 10$ V		8.0		MHz
	$V_{DD} = 15$ V		8.5		MHz
Signal Input Capactance			8.0		pF
Signal Output Capacitance	$V_{DD} = 10$ V		8.0		pF
Feedthrough Capacitance	$V_C = 0$ V		0.5		pF
Control Input Capacitance			5.0	7.5	pF

"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and cal Characteristics" provide conditions for actual device operation.

$V_{SS} = 0$ V unless otherwise specified.

These devices should not be connected to circuits with the power "ON".

In all cases, there is approximately 5 pF of probe and jig capacitance in the output; however, this capacitance is included in C_L unless specified.

V_{IS} is the voltage at the in/out pin and V_{OS} is the voltage at the out/in pin. V_C is the voltage at the control input.

Conditions for V_{IHC}:
a) $V_{IS} = V_{DD}$, I_{OS} = standard B series I_{OH} b) $V_{IS} = 0$ V, I_{OL} = standard B series I_{OL}.

Test Circuits and Switching Time Waveforms

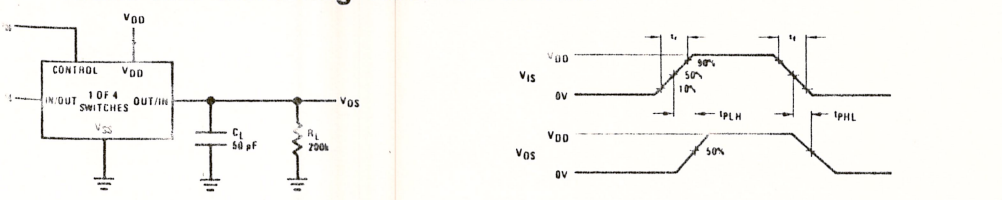


FIGURE 1. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output

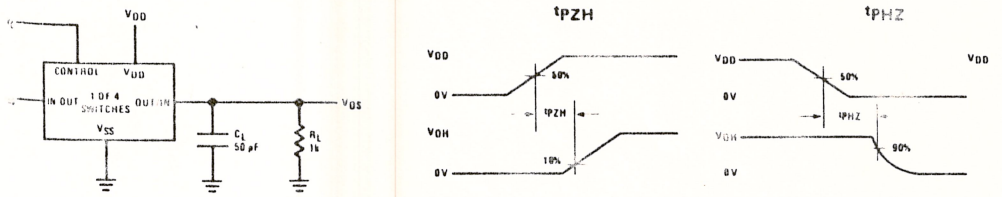


FIGURE 2. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output

tPZL tPLZ

AC Test Circuits and Switching Time Waveforms (Cont'd.)

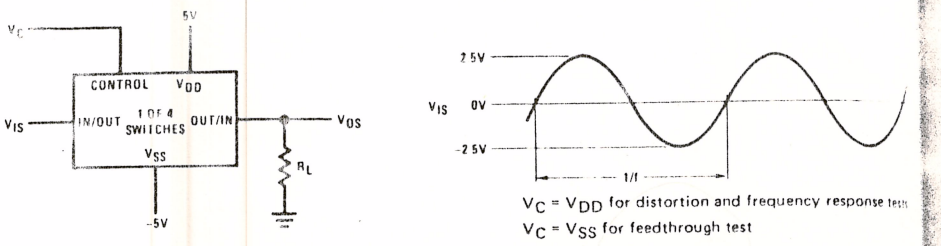


FIGURE 4. Sine Wave Distortion, Frequency Response and Feedthrough

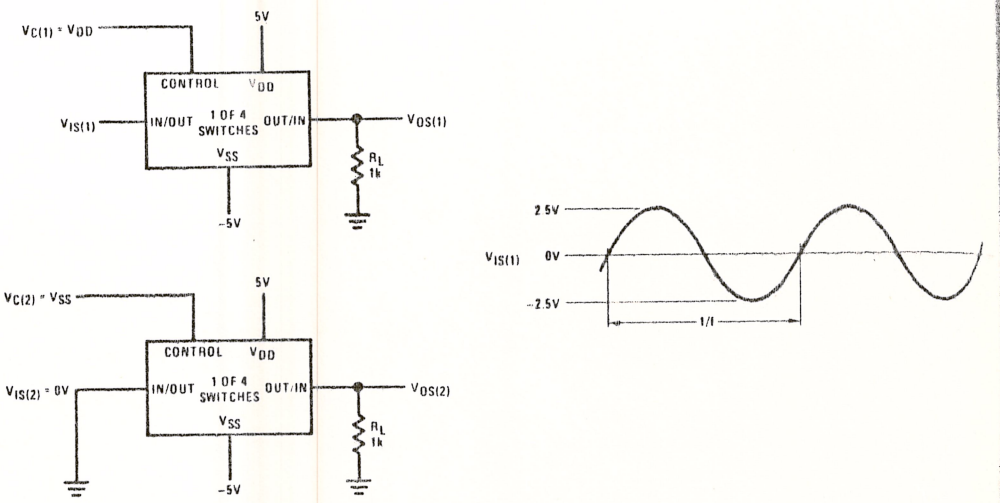


FIGURE 5. Crosstalk Between Any Two Switches

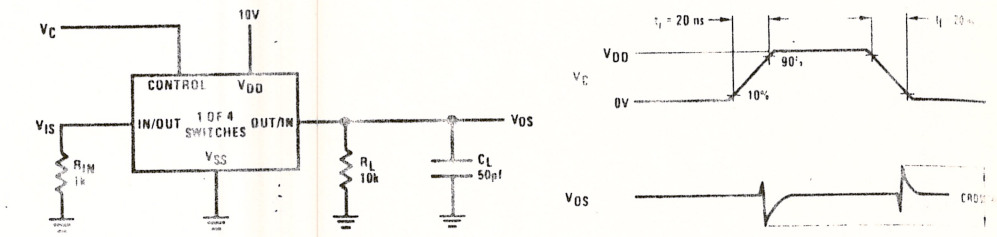


FIGURE 6. Crosstalk: Control Input to Signal Output

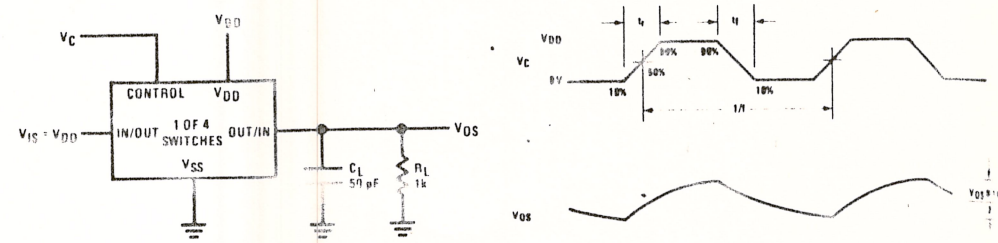
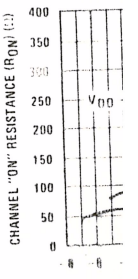


FIGURE 7. Maximum Control Input Frequency

Typical Performan

"ON" Re
Voltage



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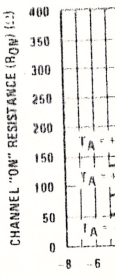


Special Consider

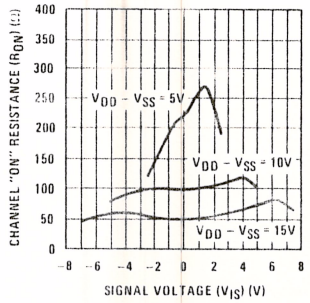
In applications where the signal to drive V_{DD} and the sig capability should exceed external load of the 4 CD4 switches). This provision a flow or clamp action on th applied or removed fro

In certain applications, the may include both V_{DD} an

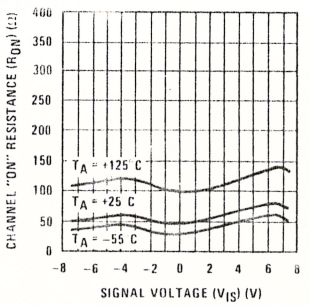
requency response tests

Typical Performance Characteristics

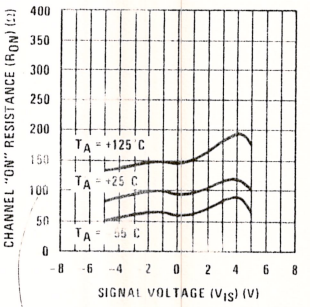
"ON" Resistance vs Signal Voltage for $T_A = 25°C$



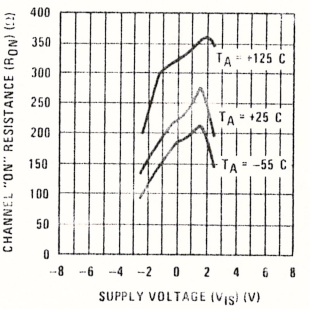
"ON" Resistance as a Function of Temperature for $V_{DD} - V_{SS} = 15V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{SS} = 10V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{SS} = 5V$



Special Considerations

In applications where separate power sources are used to drive V_{DD} and the signal input, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load of the 4 CD4066BM/CD4066BC bilateral switches). This provision avoids any permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from CD4066BM/CD4066BC.

In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 4, 8 or 11, the voltage drop across the bidirectional switch must not exceed 0.6V at $T_A \leq 25°C$, or 0.4V at $T_A > 25°C$ (calculated from R_{ON} values shown).

No V_{DD} current will flow through R_L if the switch current flows into terminals 2, 3, 9 or 10.

t_f - 20 ns

CROSSTALK