Line Modulator (see Fig.11)

Associated Register: – None

Associated flags in other registers:

$\overline{75}$/1200	–	D5	–	R2 (mode)	– transmit baud rate select.
LTXEN	–	D6	–	R3 (command)	– line transmitter/modulator output enable.

Associated Pins:	TXDATA	–	I/O	– modulator input (also (on chip) transmitter output).
	FSKOUT	–	output	– line modulator output

Operation

The modulator generates a pseudo analogue signal from a serial shift register which is parallel loaded with patterns from an internal ROM. The frequency of the sine wave is determined by the selected baud rate $\overline{75}$/1200, and the value of the data on TXDATA (pin 6).

data	'1'	'0'
1200 baud	1300 Hz	2100 Hz
75 baud	390 Hz	450 Hz

One sine wave cycle is comprised of a 92-bit pattern which after minimal external low pass filtering provides a suitable F.S.K. signal out (see Fig.11)

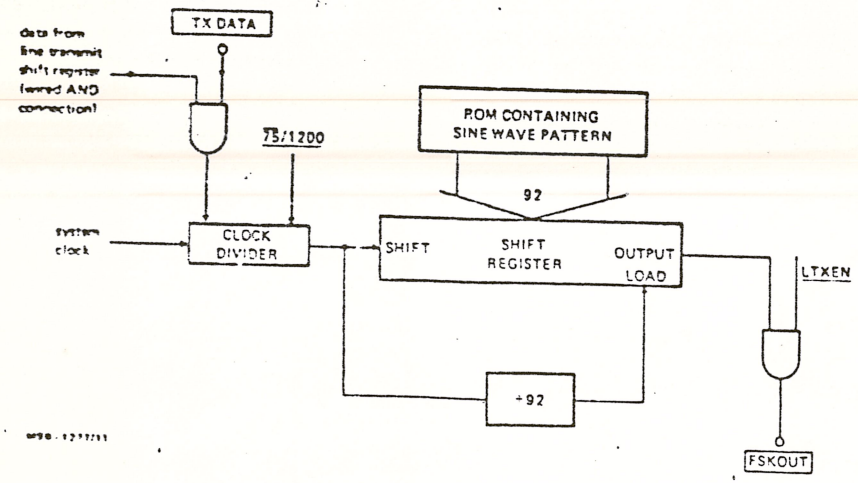


Fig.11 Line modulator block diagram

Tape section (see Fig.12)

Associated registers: – R5 – Consists of two registers with the same address:
transmit holding register write only
receive holding register read only

Associated flags in other registers:

TTXRDY	–	D7	–	R1 (status)	– transmit holding register ready to accept new data
TRXRDY	–	D6	–	R1 (status)	– valid data available in receive holding register
TDCD	–	D5	–	R1 (status)	– tape data carrier detect flag
TFERR	–	D4	–	R1 (status)	– tape framing error (derived from STOP bit of message)
TPERR	–	D3	–	R1 (status)	– tape parity error
TPO/$\overline{E}$	–	D3	–	R2 (mode)	– odd or even parity mode select.
$\overline{TPEN}$	–	D2	–	R2 (mode)	– 8-bit data or 7-bit plus parity mode select
TRXEN	–	D3	–	R3 (command)	– tape receiver enable
$\overline{TTXEN}$	–	D2	–	R3 (command)	– tape transmitter enable

Associated pins:	TFSKIN	–	input	– F.S.K. input to tape sections
	TFSKOUT	–	output	– F.S.K. modulated data out

Operation of tape section (see Fig.12)

The tape data modulation system is a modified form of the 'Kansas City' standard. A logic '1' is represented by one cycle of 1300 Hz, and a logic '0' by two cycles of 2600 Hz, the data rate being 1300 baud. The data format is the same as that for viewdata, i.e. 10-bit words consisting of a START bit (LOW), followed by 8 data bits, the 8th being an optional parity bit, ending with a STOP bit (HIGH) which is continuous until the next data word.

To operate the tape section the required parity mode should first be set up by writing the required states of TPEN and TPO/$\overline{E}$ to the mode register (R2). The TTXEN command enables the output of the transmit shift register into the modulator, and should be set before data is written to the transmit holding register. (With TTXEN = '0' the modulator outputs a continuous 1300 Hz signal '1'). When a data word is written to the transmit holding register the TTXRDY flag is reset to '0'. If the transmit shift register is not currently active the contents of the holding register, along with valid parity bit (if enabled) and the START and STOP bits are transferred to the transmit shift register, at the same time TTXRDY is set to '1'. The holding register is then free to accept new data but this will not be transferred to the shift register until the current data has been clocked out. Data should be written to the tape transmit holding register, therefore, only when TTXRDY = '1'.

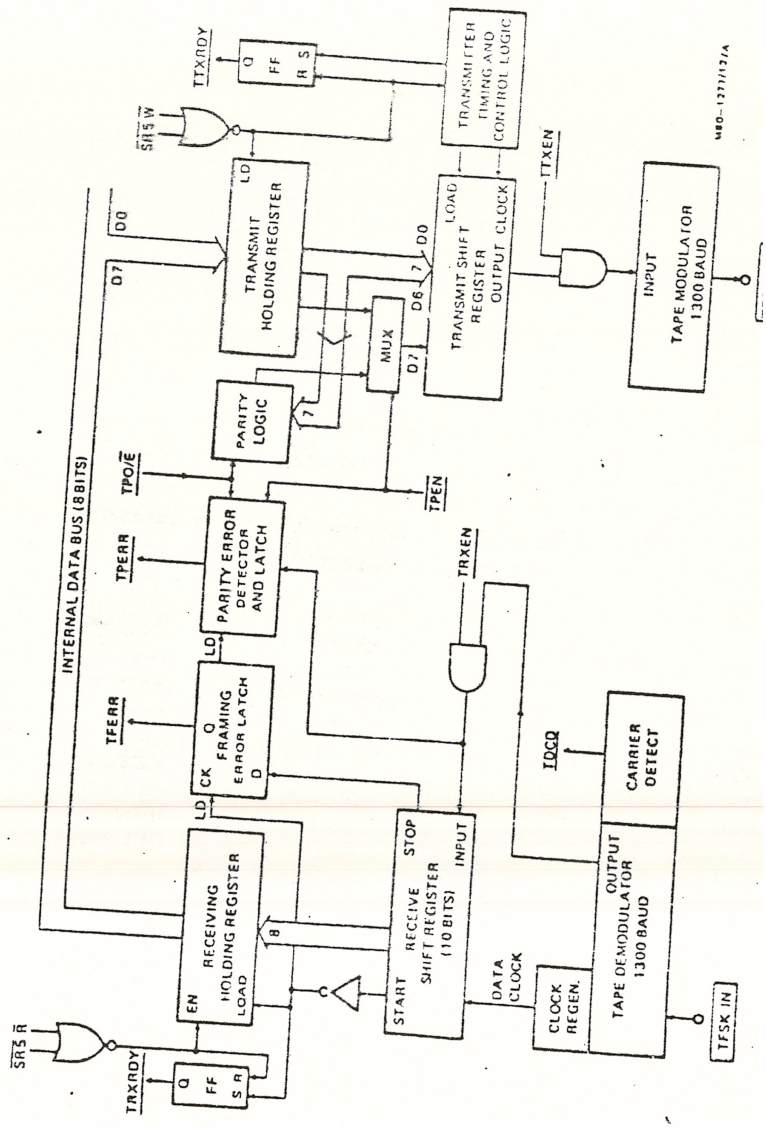
The modulator produces 1300 Hz and 2600 Hz signals which occur synchronously with the data from the transmitter. Hence a '1' is one complete 1300 Hz cycle, and a '0' two complete 2600 Hz cycles. The modulator output, TFSKOUT, requires minimal external low pass filtering to produce data suitable for audio cassette tape recorders.

To overcome the tendency of cassette recorders to attenuate high frequencies, the 1300 Hz signal contains 2 μs wide attenuating pulses every 12 μs. This reduces the 1300 Hz signal by approximately 3 dB relative to the 2600 Hz signal after external filtering.

The data rate of 1300 baud is slightly faster than the 1200 baud line receive rate, allowing incoming data from the line to be transferred simultaneously (via the microprocessor) to tape.

The TFSKIN input accepts the previously filtered and squared data from the tape recorder. The demodulator uses the fact that the modulated data is in phase with clock to regenerate the clock from the data. This permits a wide tolerance on replay speeds. A carrier detect circuit is included which sets the TDCD flag to '1' if carrier (1300 Hz or 2600 Hz) is valid for 100 ms. If carrier is lost for 100 ms the TDCD flag is reset to '0'. This flag may be read by the microprocessor to determine when to enable the tape receiver by setting TRXEN to '1'.

If TRXEN is set, then on detection of a start bit (LOW) data is shifted into the tape receive shift register by the clock which has been extracted from the data. After ten clocks, the contents of the shift register are transferred to the receive holding register. At the same time the complement of the STOP bit is loaded into the TFERR latch, the results of the parity calculation loaded into the TPERR latch, and TRXRDY is set to '1'. The TRXRDY flag is read by the microprocessor to identify when valid data is in the holding register and is reset to '0' when the holding register (R5) is read.



DEVELOPMENT SAMPLE DATA

IBUS A receiver and IBUS B receiver/transmitter (see Fig.13)

Associated registers:

Receiver A (2 bytes)	–	R10	– read only
Receiver B (2 bytes)	–	R11	– read only
Transmitter B (2 bytes)	–	R11	– write only

Associated flags in other registers:

IBRXRDY	–	D1	– R0 (status)	–	valid data available in receiver B holding register
IBTXRDY	–	D0	– R0 (status)	–	transmitter B holding register ready to accept new data
IARXRDY	–	D1	– R1 (status)	–	valid data available in receiver A holding register
CLCK IN/$\overline{\text{OUT}}$	–	D1	– R3 (command)	–	input/output control for 62.5 kHz pin
$\overline{\text{DLEN}}$ A/$\overline{\text{DLIM}}$ A	–	D0	– R3 (command)	–	3-line/2-line control for IBUS A receiver.

Associated pins:

$\overline{\text{DATA}}$ A	– input	–	receiver A data input
DLIM A/$\overline{\text{DLEN}}$ A	– input	–	receiver A data clock or bus enable signal
$\overline{\text{DATA}}$ B	– I/O	–	receiver B data input/transmitter B data output
DLIM B	– I/O	–	receiver B data clock input/transmitter B data clock output
$\overline{\text{DLEN}}$ B	– I/O	–	receiver B bus enable input/transmitter B bus enable output
IBCLCK	– I/O	–	62.5 kHz clock input/output

Operation

All three IBUS circuits (receiver A, receiver B, and transmitter B) are capable of handling variable length codes from 1 to 12 bits. (In fact 15 bits can be transmitted 12 being data the rest being trailing zero's, and 15 bits may be received but only the last 12 being retained). Each of the three circuits have two 8-bit registers which are accessed by two successive read or write operations to the same address. There is a pointer for each pair of registers which selects the first or second byte. The pointers act in a bistable fashion with each access and are reset to point to the first byte with power on, D5 set in R3, or by reading either of the status registers R0 and R1. The two bytes of data in each holding register contain 12 bits of message, and 4-bits which specify the word length of message. For the transmitter the word length is used to generate the correct number of data clocks, for the receivers it may be used to identify the source of the message, or to establish that the message was a valid length.

The contents of each receiver register pair is organised as:

1st byte	D7	D6	D5	D4	D3	D2	D1	D0
RXA – R10A RXB – R11A	L – 4	L – 5	L – 6	L – 7	L – 8	L – 9	L – 10	L – 11

2nd byte	D7	D6	D5	D4	D3	D2	D1	D0
RXA – R10B RXB – R11B	Word length MSB	Word length	Word length	Word length LSB	L	L – 1	L – 2	L – 3

Where L, L – 1 etc. means last data bit received, last minus one etc.

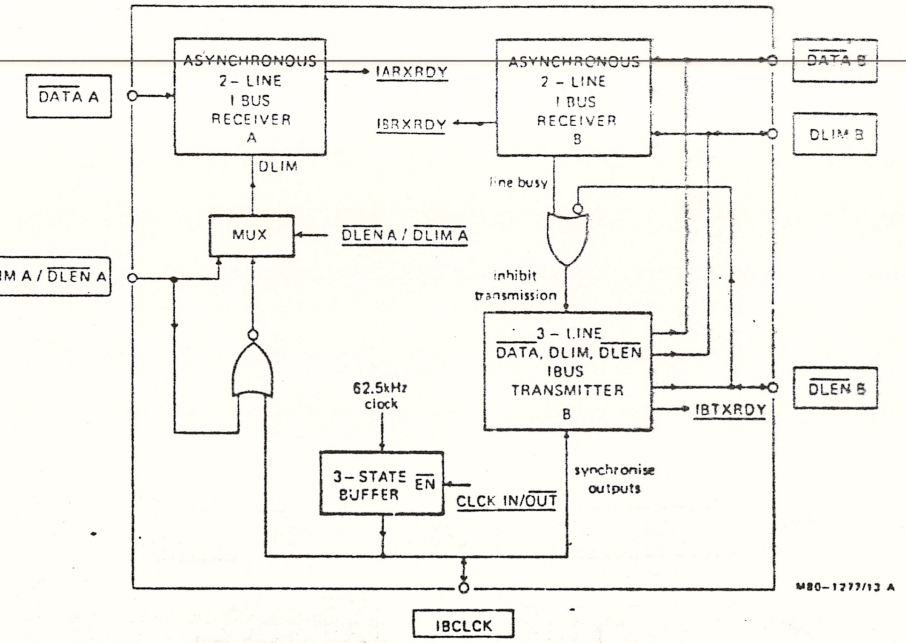


Fig.13 IBUS block diagram

or the transmitter the register pair is organised as:

st byte	D7	D6	D5	D4	D3	D2	D1	D0
XB – R11A	8	7	6	5	4	3	2	1

nd byte	D7	D6	D5	D4	D3	D2	D1	D0
(B – R11B	Word length MSB	Word length	Word length	Word length LSB	12	11	10	9

Where 1, 2, etc. means first data bit transmitted, second data bit transmitted, etc.

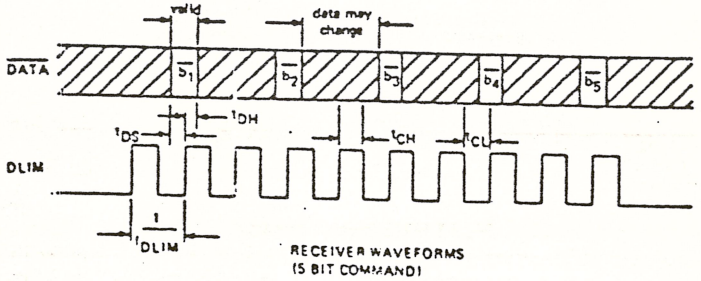
IARXRDY or IBRXRDY (D1 in status registers R1 and R0) are set when a message has been received by RXA or RXB respectively. These flags also inhibit the receive holding registers from being overwritten by subsequent messages until the holding registers have been read. Reading a holding register pair will reset the relevant IARXRDY or IBRXRDY flags.

Transmitter B is initiated by writing two bytes to the transmit holding register (R11). This sets IBTXRDY to '0'. The DLIM line is sampled to detect the line busy state, and when the line is free a time out starts. If further DLIM's are detected before the end of the time out period the time out is reset and the sequence will begin again. When the time out has been completed the contents of the holding register are transferred to the output shift register and word length counter. The data and correct number of data clocks are then transmitted, at the completion of which IBTXRDY is returned to a '1'. New data should not be written to the transmit holding register (R11) while IBTXRDY = '0'. If the line is busy when a transmission is requested, the transmission will not start until 300 – 330 μs after the line becomes free (last DLIM).

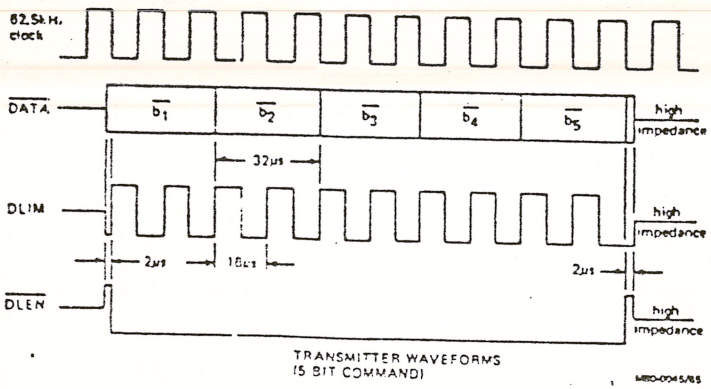
Receiver B is inhibited from receiving data transmitted by transmitter B.

Receiver A may operated either as a two line receiver with DATA and DLIM, or as a three line $\overline{\text{DATA}}$, $\overline{\text{DLEN}}$ and CLK receiver. DLIM A/$\overline{\text{DLEN}}$ A use the same pin, the function of which is selected by the $\overline{\text{DLEN}}$ A/DLIM A command D0, register R3 (command).

The 62.5 kHz clock (pin IBCLCK) may be used either as an input for receiver A (as described above), or to synchronise transmitter B outputs, or as an output synchronous with transmitter B. The functior is selected by CLCK IN/$\overline{\text{OUT}}$ command D1 in R3



RECEIVER WAVEFORMS (5 BIT COMMAND)



TRANSMITTER WAVEFORMS (5 BIT COMMAND)

Fig. 14 IBUS waveforms

DEVELOPMENT SAMPLE DATA

PORT A

Associated register: R6 – bits 0 to 4 – read/write

Associated pins: PA0 to PA4

Operation

This is a 5-bit general purpose input/output port. The outputs are latched and are open drain up to nominal 12 V.

The latches may be accessed by the microprocessor via BUS D0 to D7 by a read or write sequence to register R6. If any pin of the port is used as an input then its output latch must first be written with a '1'. This allows the external circuit to control the pin. The state of the pins may be read by the microprocessor by reading R6. If the supply to the open drain outputs is turned on before the V_{DD} supply to the IC, then the PORT must first be cleared by writing 1's to the output latch before operation.

PORT A might typically be used in viewdata mode as an interface to a non-volatile memory in which telephone and password numbers may be stored.

PORT B

Associated register: R7 – bits 0 to 3 – read/write

Associated pins: PB0 to PB3

Operation

This is a 4-bit general purpose input/output port. It behaves in exactly the same way as PORT A except that access is by addressing R7, and that outputs PB1 to PB3 are open drain to nominal 12 V, and might typically be used in combined teletext/viewdata applications to control the Picture On function.

Mullard

APPENDIX
Register map

	D7	D6	D5	D4	D3	D2	D1	D0	
R0	LTXRDY R	LRXRDY R	LDCD R	LFERR R	LPERR R	LIDCD R	IBRXRDY R	IBTXRDY R	STATUS REGISTER 0
R1	TTXRDY R	TRXRDY R	TDCD R	TFERR R	TPERR R		IARXRDY R		STATUS REGISTER 1
R2	LPO/$\overline{E}$ R/W	$\overline{\text{LPEN}}$ R/W	$\overline{75}$/1200 R/W		TPO/$\overline{E}$ R/W	$\overline{\text{TPEN}}$ R/W			MODE REGISTER
R3	LRXEN R/W	LTXEN R/W	RESET R/W	LOBEN R/W	TRXEN R/W	TTXEN R/W	CLCK IN/$\overline{\text{OUT}}$ R/W	$\overline{\text{DLEN A}}$/$\overline{\text{DLIM A}}$ R/W	COMMAND REGISTER
R4 R	PARITY OR B8 (R)	B7 R	B6 R	B5 R	B4 R	B3 R	B2 R	B1 R	LINE RECEIVE HOLDING REGISTER
R4 W	PARITY OR B8 (W)	B7 W	B6 W	B5 W	B4 W	B3 W	B2 W	B1 W	LINE TRANSMIT HOLDING REGISTER
R5 R	PARITY OR B8 (R)	B7 R	B6 R	B5 R	B4 R	B3 R	B2 R	B1 R	TAPE RECEIVE HOLDING REGISTER
R5 W	PARITY OR B8 (W)	B7 W	B6 W	B5 W	B4 W	B3 W	B2 W	B1 W	TAPE TRANSMIT HOLDING REGISTER
R6				PA4 R/W	PA3 R/W	PA2 R/W	PA1 R/W	PA0 R/W	PORT A
R7					PB3 R/W	PB2 R/W	PB1 R/W	PB0 R/W	PORT B
R8	UK/$\overline{\text{EUR}}$ R/W	60s TIMER R/W	DIAL GO R/W	1.5s TIMER R/W	DI3 W	DI2 W	DI1 W	DI0 W	DIAL CONTROL AND TIMING REGISTER
R10 A	B8 R	B7 R	B6 R	B5 R	B4 R	B3 R	B2 R	B1 R	IBUS A REGISTERS
R10 B	– WL3 R	– WL2 R	– WL1 R	– WL0 R	– B12 R	– B11 R	– B10 R	– B9 R	

DEVELOPMENT SAMPLE DATA

APPENDIX
Register map (continued)

	D7	D6	D5	D4	D3	D2	D1	D0	
R11 A	B8 R/W	B7 R/W	B6 R/W	B5 R/W	B4 R/W	B3 R/W	B2 R/W	B1 R/W	IBUS B REGISTERS
R11 B	– WL3 R/W	– WL2 R/W	– WL1 R/W	– WL0 R/W	– B12 R/W	– B11 R/W	– B10 R/W	– B9 R/W	

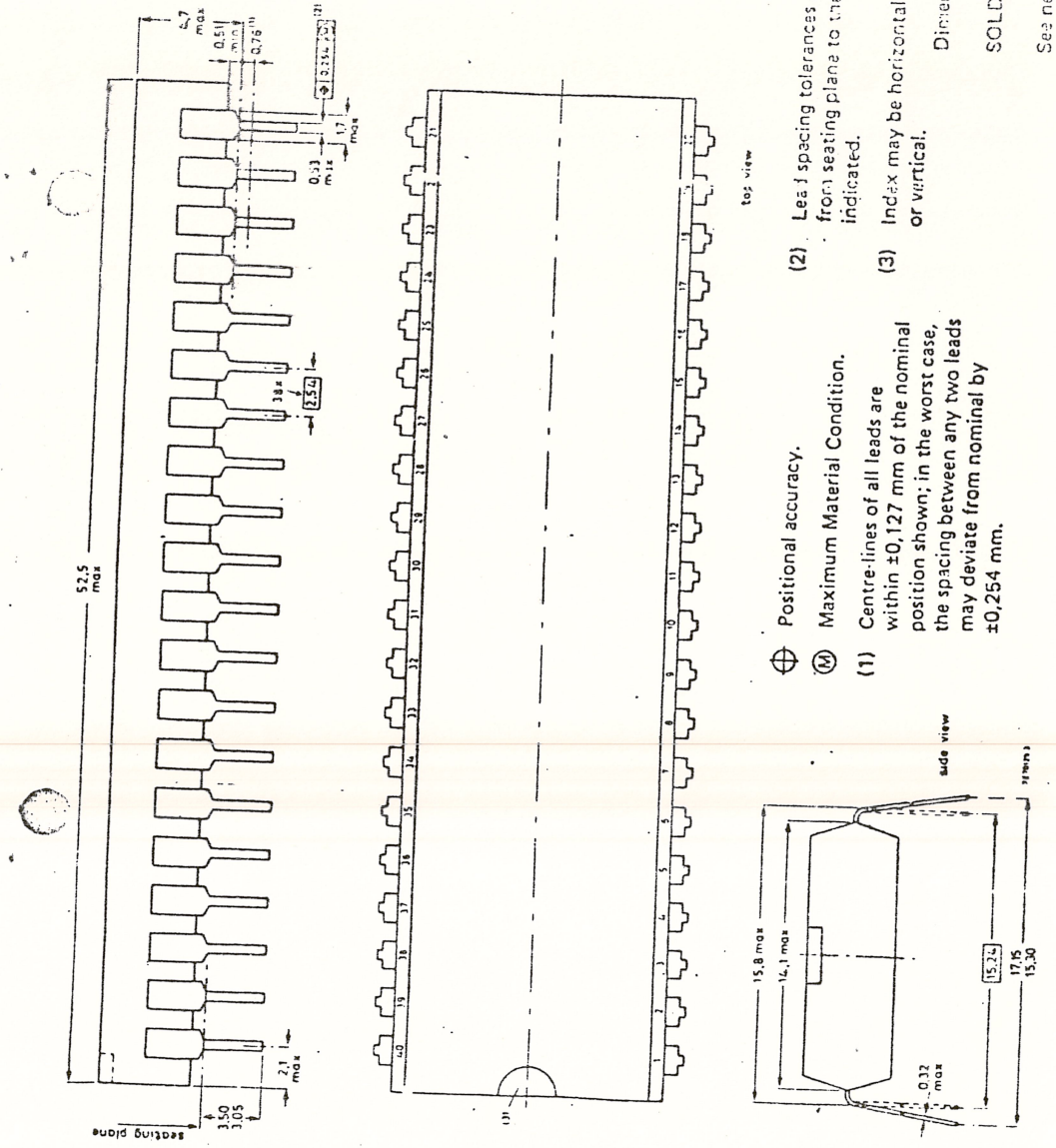
NOTE R9 is unused.

For details of bit movement in R10 and R11 see discussion of IBUS operation. A mnemonic list for use with this register map and Fig.1b is given on the next page.

MNEMONIC LIST

ALE	address latch enable from microprocessor
CLCK IN/$\overline{\text{OUT}}$	input/output control for 62.5 kHz clock pin
CPNTR	pointer signal for two byte registers
$\overline{\text{DLEN}}$ A/$\overline{\text{DLIM}}$ A	three line/two line control for IBUS A receiver
DON	dial off normal relay control for dialling
IMP	impulsing relay control for dialling
IARXRDY	IBUS A receiver ready — data available
IBRXRDY	IBUS B receiver ready — data available
IBTXRDY	IBUS B transmitter ready — previous transmission complete
LDBEN	line demodulator output buffer enable
LDCD	line data carrier detected
LFERR	line receiver framing error — received stop bit not HIGH
LIDCD	line instantaneous data carrier detect
$\overline{\text{LPEN}}$	line parity enable command
LPERR	line receiver parity error flag
LPO/$\overline{\text{E}}$	line parity odd/even command
LRXEN	line receiver enable
LRXRDY	line receiver ready — data available
LTXEN	line transmitter and modulator enable
LTXRDY	line transmitter ready — transmit holding register empty
$\overline{\text{SR}}n	select register 'n'
TDCD	tape data carrier detected
TFERR	tape receiver framing error — received stop bit not HIGH
$\overline{\text{TPEN}}$	tape parity enable command
TPERR	tape receiver parity error flag
TPO/$\overline{\text{E}}$	tape parity odd/even command
TRXEN	tape receiver enable
TRXRDY	tape receiver ready — data available
TTXEN	tape transmitter enable
TTXRDY	tape transmitter ready — transmit holding register empty
UK/$\overline{\text{EUR}}$	impulsing ratio control for UK and European standards
$\overline{75}$/1200	baud rate selection command for line modulator and line transmit shift register

40-LEAD DUAL IN-LINE; PLASTIC (SOT-129)



SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.