TABLE 14. WRITE DELETED DATA

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	0	0	1	0	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	← C →								Sector ID information prior to command execution. The four bytes are compared against header on floppy disk.
	W	← H →								
	W	← R →								
	W	← N →								
	W	← EOT →								
	W	← GPL →								
	W	← DTL →								
EXECUTION										Data transfer between FDD and main system.
RESULTS	R	← ST0 →								Status information after command execution.
	R	← ST1 →								
	R	← ST2 →								
	R	← C →								Sector ID information after command execution.
	R	← H →								
	R	← R →								
	R	← N →								

TABLE 15. READ A TRACK

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	MF	SK	0	0	0	1	0	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	← C →								Sector ID information prior to command execution.
	W	← H →								
	W	← R →								
	W	← N →								
	W	← EOT →								
	W	← GPL →								
	W	← DTL →								
EXECUTION										Data transfer between FDD and main system. FDD reads all data fields from index hole to EOT.
RESULTS	R	← ST0 →								Status information after command execution.
	R	← ST1 →								
	R	← ST2 →								
	R	← C →								Sector ID information after command execution.
	R	← H →								
	R	← R →								
	R	← N →								

TABLE 16. READ ID

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	MF	0	0	1	0	1	0	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
EXECUTION										The first correct ID information on the cylinder is stored in Data Register.
RESULTS	R	← ST0 →								Status information after command execution.
	R	← ST1 →								
	R	← ST2 →								
	R	← C →								Sector ID information read during Execution Phase from floppy disk.
	R	← H →								
	R	← R →								
	R	← N →								

TABLE 17. FORMAT A TRACK

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	MF	0	0	1	1	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	← N →								Bytes/Sector
	W	← SC →								Sectors/Track
	W	← GPL →								Gap 3
	W	← D →								Filler Byte
EXECUTION										Floppy Disk Controller (FDC) formats an entire track.
RESULTS	R	← ST0 →								Status information after command execution.
	R	← ST1 →								
	R	← ST2 →								
	R	← C →								In this case, the ID information has no meaning.
	R	← H →								
	R	← R →								
	R	← N →								

TABLE 18. SCAN EQUAL

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	1	0	0	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	← C →								Sector ID information prior to command execution.
	W	← H →								
	W	← R →								
	W	← N →								
	W	← EOT →								
	W	← GPL →								
	W	← STP →								
EXECUTION										Data compared between the FDD and main system.
RESULTS	R	← ST0 →								Status information after command execution.
	R	← ST1 →								
	R	← ST2 →								
	R	← C →								Sector ID information after command execution.
	R	← H →								
	R	← R →								
	R	← N →								

TABLE 19. SCAN LOW OR EQUAL

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	1	1	0	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	←			C				→	Sector ID information prior to command execution.
	W	←			H				→	
	W	←			R				→	
	W	←			N				→	
	W	←			EOT				→	
	W	←			GPL				→	
	W	←			STP				→	
EXECUTION										Data compared between the FDD and main system.
RESULTS	R	←			ST0				→	Status information after command execution.
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	Sector ID information after command execution.
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	

TABLE 20. SCAN HIGH OR EQUAL

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	1	1	1	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	←			C				→	Sector ID information prior to command execution.
	W	←			H				→	
	W	←			R				→	
	W	←			N				→	
	W	←			EOT				→	
	W	←			GPL				→	
	W	←			STP				→	
EXECUTION										Data compared between the FDD and main system.
RESULTS	R	←			ST0				→	Status information after command execution.
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	Sector ID information after command execution.
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	

TABLE 21. RECALIBRATE*

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	0	0	0	0	1	1	1	Command Codes
	W	X	X	X	X	X	0	US1	US0	
EXECUTION										Head retracted to Track zero.

* The WD37C65/A issues 255 step pulses as opposed to 77 for the NEC765.
The WD37C65B issues 77 step pulses, the same as the NEC765.

TABLE 22. SENSE INTERRUPT STATUS

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	0	0	0	1	0	0	0	Command Codes
RESULTS	R	←			ST0				→	Status information about the FDC at the end of seek operation.
	R	←			PCN				→	

TABLE 23. SPECIFY

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	0	0	0	0	0	1	1	Command Codes
	W	←	SRT	→		←		HUT	→	
	W	←		HLT				ND	→	

TABLE 24. SENSE DRIVE STATUS

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	0	0	0	0	1	0	0	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
RESULTS	R	←			ST3				→	Status information about the FDC.

TABLE 25. SEEK

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	0	0	0	1	1	1	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	←			NCN				→	
EXECUTION										Head is positioned over proper cylinder on the diskette.

Table 26 defines, in alphabetical order, the symbols used in Command Tables 11 through 25.

TABLE 26. COMMAND SYMBOL DESCRIPTIONS

SYMBOL	NAME	DESCRIPTION
A0	ADDRESS LINE 0	A0 controls selection of Main Status Register (A0=0) or Data Register (A0=1).
C	CYLINDER NUMBER	C stands for the current/selected cylinder (track) numbers 0 through 255 of the medium.
D	DATA	D stands for the data pattern which is going to be written into a sector.
D7 - D0	DATA BUS	8-bit DATA BUS, where D7 stands for a most significant bit, and D0 stands for a least significant bit.
DTL	DATA LENGTH	When N is defined as 00, DTL stands for the DATA LENGTH which users are going to read out or write into the sector.

TABLE 26. COMMAND SYMBOL DESCRIPTIONS (cont.)

SYMBOL	NAME	DESCRIPTION
EOT	END OF TRACK	EOT stands for the final sector number on a cylinder. During Read or Write operations, FDC will stop data transfer after a sector number equal to EOT.
GPL	GAP LENGTH	GPL stands for the length of Gap 3. During the FORMAT Command, it determines the size of Gap 3.
H	HEAD ADDRESS	H stands for head number 0 or 1, as specified in the ID field.
HLT	HEAD LOAD TIME	HLT stands for the HEAD LOAD TIME in FDD (2 to 254ms in 2ms increments).
HS	HEAD SELECT	HS stands for a selected head number 0 or 1 and controls the polarity of pin 25 (in 40 pin DIP) or pin 28 (in 44 pin PLCC).
HUT	HEAD UNLOAD TIME	HUT stands for the HEAD UNLOAD TIME after a Read or Write operation has occurred (16 to 240ms in 16ms increments).
MF	FM or MFM	If MF is low, FM mode is selected. If it is high, MFM mode is selected.
MT	MULTITRACK	If MT is high, a MULTITRACK operation is performed. If MT=1 after finishing Read/Write operation on side 0, FDC will automatically start searching for sector 1 on side 1.
N	NUMBER	N stands for the NUMBER of data bytes written in a sector.
NCN	NEW CYLINDER NUMBER	NCN stands for a NEW CYLINDER NUMBER which is going to be reached as a result of the Seek operation. Desired position of head.
ND	NON-DMA MODE	ND stands for operation in the NON-DMA MODE.
PCN	PRESENT CYLINDER	PCN stands for the cylinder number at the completion of the SENSE INTERRUPT STATUS Command. Position of head at present time.
R	RECORD	R stands for the sector number which will be read or written.
R/W	READ/WRITE	R/W stands for either READ or WRITE signal.
SC	SECTOR	SC indicates the number of sectors per cylinder.
SK	SKIP	SK stands for SKIP Deleted Data Address mark.
SRT	STEP RATE TIME	SRT stands for the Stepping Rate for the FDD (1 to 16ms in 1ms increments). Stepping Rate applies to all drives. In 2's complement format, F(Hex)=1ms, E(Hex)=2ms, etc.
ST0 ST1 ST2 ST3	STATUS 0 STATUS 1 STATUS 2 STATUS 3	ST0 – 3 stands for one of four registers which store the STATUS information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the Main Status Register (selected by A0=0). ST0 – 3 may be read only after a command has been executed and contains information relevant to that particular command.
STP		During a SCAN operation, if STP=1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); if STP=2, then alternate sectors are read and compared.
US0,US1	UNIT SELECT	US stands for a selected drive; binary encoded, 1 of 4.

COMMAND DESCRIPTIONS

Read Data

A set of nine byte words are required to place the FDC into the Read Data Mode. After the Read Data command has been issued, the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading ID Address Marks and ID fields. When the current sector number ("R") stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC outputs data (from the data field) byte-to-byte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a "Multi-sector Read Operation." The Read Data Command may be terminated by the receipt of a Terminal Count signal. TC should be issued at the same time that the $\overline{DACK}$ for the last byte of data is sent. Upon receipt of this signal, the FDC stops outputting data to the processor, but will continue to read data from the current sector, check CRC (Cyclic Redundancy Count) bytes, and then at the end of the sector terminate the Read Data command. The amount of data which can be handled with a single command to the FDC depends upon MT (multitrack), MF (MFM/FM), and N (number of bytes/sector). Table 27 lists the Transfer Capacity.

TABLE 27. TRANSFER CAPACITY

Multi-Track MT	MFM/FM MF	Bytes/Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Diskettes
0	0	00	(128) (26) = 3,328	26 at Side 0
0	1	01	(256) (26) = 6,656	or 26 at Side 1
1	0	00	(128) (52) = 6,656	26 at Side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at Side 0
0	1	02	(512) (15) = 7,680	or 15 at Side 1
1	0	01	(256) (30) = 7,680	15 at Side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at Side 0
0	1	03	(1024) (8) = 8,192	or 8 at Side 1
1	0	02	(512) (16) = 8,192	8 at Side 1
1	1	03	(1024) (16) = 16,384	

The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing at Sector L, Side 1 (Sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, then DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a sector, the data beyond DTL in the sector is not sent to the Data Bus. The FDC reads (internally) the complete sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read operation. When N is non-zero, then DTL has no meaning and should be set to FF hexidecimal.

At the completion of the Read Data command, the head is not unloaded until after Head Unload Time Interval (specified in the Specify command) has elapsed. If the processor issues another command before the head unloads, then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC detects the Index Hole twice without finding the right sector, (indicated in 'R'), then the FDC sets the ND (No Data) flag in Status Register 1 to a 1 (high), and terminates the Read Data command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the DE (Data Error) flag in Status Register 1 to 1 (high). If a CRC error occurs in the Data Field, the FDC also sets the DD (Data Error in Data Field) flag in Status Register 2 to a 1 (high), and terminates the Read Data command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

If the FDC reads a Deleted Data Address Mark off the diskette, and the SK bit (bit D5 in the first Command Word) is not set (SK = 0), then the FDC sets the CM (Control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data command, after reading all the data in the sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector. The CRC bits in the deleted data field are not checked when SK = 1.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be serviced by the processor every 27 μs in the FM mode, and every 13 μs in the MFM mode, or the FDC sets the OR (Overrun) flag in Status Register 1 to a 1 (high), and terminates the Read Data command.

If the processor terminates a read (or write) operation in the FDC, then the ID information in the Result phase is dependent upon the state of the MT bit and EOT byte. Table 28 shows the values for C, H, R, and N, when the processor terminates the command.

TABLE 28. C, H, R, AND N VALUES

MT	HD	Final Sector Transferred to Processor	ID Information at Result Phase C	H	R	N
0	0	Less than EOT	NC	NC	R+1	NC
	0	Equal to EOT	C+1	NC	R=01	NC
	1	Less than EOT	NC	NC	R+1	NC
	1	Equal to EOT	C+1	NC	R=01	NC
1	0	Less than EOT	NC	NC	R+1	NC
	0	Equal to EOT	NC	LSB	R=01	NC
	1	Less than EOT	NC	NC	R+1	NC
	1	Equal to EOT	C+1	LSB	R=01	NC

Notes: NC (No Change): The same value as the one at the beginning of command execution. LSB (Least Significant Bit): The least significant bit of H is complemented.

Write Data

A set of nine bytes is required to set the FDC into the Write Data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify command), and begins reading ID fields. When all four bytes loaded during the command (C, H, R, N) match the four bytes of the ID field from the diskette, the FDC takes data from the processor byte-by-byte via the data bus and outputs it to the FDD.

After writing data into the current sector, the sector number stored in 'R' is incremented by one, and the next data field is written into. The FDC continues this 'Multisector Write Operation' until the issuance of a Terminal Count signal. If a Terminal Count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written, then the remainder of the data field is filled with zeros.

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (CRC error) in one of the ID fields, it sets the DE (Data Error) flag of Status Register 1 to a 1 (high) and terminates the Write Data command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

The Write command operates in much the same manner as the Read command. The following items are the same, and one should refer to the Read Data command for details:

- Transfer capacity
- EN (End of Cylinder) flag
- ND (No Data) flag
- Head Unload Time interval
- ID Information when the processor terminates command
- Definition of DTL when N = 0 and when N ≠ 0

In the Write Data mode, data transfers between the processor and FDC via the data bus, must occur every 27 μs in the FM mode and every 13 μs in the MFM mode. If the time interval between data transfers is longer than this, then the FDC sets the OR (Overrun) flag in Status Register 1 to a 1 (high) and terminates the Write Data command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

Write Deleted Data

This command is the same as the Write Data command except a Deleted Data Address mark is written at the beginning of the data field instead of the normal Data Address mark.

Read Deleted Data

This command is the same as the Read Data command except that when the FDC detects a Data Address mark at the beginning of a data field (and SK = 0 [low]), it will read all the data in the sector and set the CM flag in Status Register 2 to a 1 (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the Data Address mark and reads the next sector.

Read A Track

This command is similar to the Read Data command except that this is a continuous Read operation where the entire data field from each of the sectors is read. Immediately after sensing the index hole, the FDC starts reading all data fields on the track as continuous blocks of data. If the FDC finds an error in the ID or Data CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR and sets the ND flag of Status Register 1 to a 1 (high) if there is no comparison. Multitrack or skip operations are not allowed with this command.

This command terminates when the number of sectors read is equal to EOT. If the FDC does not find an ID Address mark on the diskette after it senses the index hold for the second time, it sets the MA (Missing Address mark) flag in Status Register 1 to a 1 (high) and terminates the command. (Status Register 0 has bits 7 and 6 set to 0 and 1 respectively.)

Read ID

The Read ID command is used to give the present position of the recording head. The FDC stores the values from the first ID field it is able to read. If no proper ID Address mark is found on the diskette before the index hole is encountered for the second time, then the MA (Missing Address mark) flag in Status Register 1 is set to a 1 (high), and if no data is found then the ND (No Data) flag is also set in Status Register 1 to a 1 (high). The command is then terminated with bits 7 and 6 in Status Register 0 set to 0 and 1 respectively. During this command there is no data transfer between FDC and the CPU except during the result phase.

Format A Track

The Format command allows an entire track to be formatted. After the index hole is detected, data is written on the diskette; Gaps, Address marks, ID fields and data fields, all per the IBM System 34 (double density) or System 3740 (single density) format are recorded. The particular format which will be written is controlled by the values programmed into N (number of bytes/sector), SC (sectors/cylinder), GPL (gap length), and D (data pattern) which are supplied by the processor during the Command phase. The data field is filled with the byte of data stored in D. The ID field for each sector is supplied by the processor; that is, four data requests per sector are made by the FDC for C (cylinder number), H (head number), R (sector number) and N (number of bytes/sector). This allows the diskette to be formatted with nonsequential sector numbers, if desired.

The processor must send new values for C, H, R, and N to the WD37C65A/B for each sector on the track. If FDC is set for the DMA mode, it will issue four DMA requests per sector. If it is set for the Interrupt mode, it will issue four interrupts per sector and the processor must supply C, H, R, and N loads for each sector. The contents of the R register are incremented by 1 after each sector is formatted, thus, the R register contains a value of R when it is read during the Result phase. This incrementing and formatting continues for the whole track until the FDC detects the index hole for the second time, whereupon it terminates the command.

Table 29 shows the relationship between N, SC, and GPL for various sector sizes.

TABLE 29. N, SC AND GPL RELATIONSHIP

Format	Sector Size	N	SC	GPL[1]	GPL[2,3]
8" Standard Floppy					
FM Mode	128 bytes/sector	00	1A	07	1B
	256	01	0F	0E	2A
	512	02	08	1B	3A
	1024	03	04	47	8A
	2048	04	02	C8	FF
	4096	05	01	C8	FF
MFM Mode[4]	256	01	1A	0E	36
	512	02	0F	1B	54
	1024	03	08	35	74
	2048	04	04	99	FF
	4096	05	02	C8	FF
	8192	06	01	C8	FF
5¼" Minifloppy					
FM Mode	128 bytes/sector	00	12	07	09
	128	00	10	10	19
	256	01	08	18	30
	512	02	04	46	87
	1024	03	02	C8	FF
	2048	04	01	C8	FF
MFM Mode[4]	256	01	12	0A	0C
	256	01	10	20	32
	512	02	08	2A	50
	1024	03	04	80	F0
	2048	04	02	C8	FF
	4096	05	01	C8	FF
3½" Sony Microfloppy					
FM Mode	128 bytes/sector	0	0F	07	1B
	256	1	09	0E	2A
	512	2	05	1B	3A
MFM Mode[4]	256	1	0F	0E	36
	512	2	09	1B	54
	1024	3	05	35	74

Notes:
1. Suggested values of GPL in Read or Write commands to avoid splice point between data field and ID field of contiguous sections.
2. Suggested values of GPL in format command.
3. All values except sector size are hexidecimal.
4. In MFM mode FDC cannot perform a Read/Write/format operation with 128 bytes/sector. (N = 00)

Scan Commands

The Scan commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system. The FDC compares the data on a byte-by-byte basis and looks for a sector of data which meets the conditions of $D_{FDD} = D_{Processor}$, $D_{FDD} \leq D_{Processor}$, or $D_{FDD} \geq D_{Processor}$. The hexidecimal byte of FF either from memory or from FDD can be used as a mask byte because it always meets the condition of the comparison. One's complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremented (R + STP → R), and the scan operation is continued. The scan operation continues until one of the following conditions occur: the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

If the conditions for scan are met, then the FDC sets the SH (Scan Hit) flag of Status Register 2 to a 1 (high) and terminates the Scan command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied) flag of Status Register 2 to a 1 (high) and terminates the Scan command. The receipt of a Terminal Count signal from the processor or DMA controller durring the scan operation will cause the FDC to complete the comparison of the particular byte which is in process and then to terminate the command. Table 30 shows the status of bits SH and SN under various conditions of Scan.

TABLE 30. STATUS OF BITS SH AND SN

Command	Status Register 2 Bit 2 - SN	Status Register 2 Bit 3 - SH	Comments
Scan Equal	0	1	$D_{FDD} = D_{Processor}$
	1	0	$D_{FDD} \neq D_{Processor}$
Scan Low or Equal	0	0	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} < D_{Processor}$
	1	0	$D_{FDD} > D_{Processor}$
	0	1	$D_{FDD} = D_{Processor}$
Scan High or Equal	0	0	$D_{FDD} > D_{Processor}$
	1	0	$D_{FDD} < D_{Processor}$

If the FDC encounters a Deleted Data Address mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets the CM (Control mark) flag of Status Register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC skips the sector with the Deleted Address mark and reads the next sector. In the second case (SK = 1), the FDC sets the CM (Control mark) flag of Status Register 2 to a 1 (high) in order to show that a deleted sector had been encountered.

When either the STP (contiguous sectors = 01, or alternate sectors = 02) sectors are read or the MT (Multitrack) is programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26 and the Scan command is started at sector 21, the following will happen: sectors 21, 23, and 25 will be read, then the next sector (26) will be skipped and the index hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the Scan command would be completed in a normal manner.

During the Scan command, data is supplied by either the processor or DMA controller for comparison against the data read from the diskette. In order to avoid having the OR (Overrun) flag set in Status Register 1, it is necessary to have the data available in less than 27 μs (FM mode) or 13 μs (MFM mode). If an Overrun occurs, the FDC ends the command with bits 7 and 6 of Status Register 0 set to 0 and 1, respectively.

Seek

The Read/Write head within the FDD is moved from cylinder to cylinder under control of the Seek command. FDC has four independent Present Cylinder Registers for each drive. They are cleared only after the Recalibrate command. The FDC compares the PCN (Present Cylinder Number) which is the current head position with the NCN (New Cylinder Number), and if there is a difference, performs the following operations:

PCN < NCN: Direction signal to FDD set to a 1 (high), and step pulses are issued. (Step In)

PCN > NCN: Direction signal to FDD set to a 0 (low), and step pulses are issued. (Step Out)

The rate at which step pulses are issued is controlled by SRT (Stepping Rate Time) in the Specify command. After each step pulse is issued NCN is compared against PCN, and when NCN = PCN, the SE (Seek End) flag is set in Status Register 0 to a 1 (high), and the command is terminated. At this point FDC interrupt goes high. Bits D_0B–D_3B in the Main Status Register are set during the Seek operation and are cleared by the Sense Interrupt Status command.

During the command phase of the Seek operation the FDC is in the FDC Busy state; but during the Execution phase, it is in the non-busy state. While the FDC is in the non-busy state, another Seek command may be issued, and in this manner parallel Seek operations may be done on up to four drives at once. No other command can be issued for as long as the FDC is in the process of sending step pulses to any drive.

If the time to write three bytes of Seek command exceeds 150µs, the timing between the first two step pulses may be shorter than set in the Specify command by as much as 1ms.

Recalibrate

The function of this command is to retract the Read/Write head within the FDD to the Track 0 position. The FDC clears the contents of the PCN counter and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is low, the Direction signal remains 0 (low) and step pulses are issued. When the Track 0 signal goes high, the SE (Seek End) flag in Status Register 0 is set to a 1 (high) and the command is terminated. If the Track 0 signal is still low after 255 step pulses have been issued, (for the WD37C65 and the WD37C65A) or 77 step pulses (WD37C65B), the FDC sets the SE (Seek End) and EC (Equipment Check) flags of Status Register 0 to both 1s (highs), and terminates the command after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively.

The ability to do overlap Recalibrate commands to multiple FDDs and the loss of the Ready signal, as described in the Seek command, also applies to the Recalibrate command.

Sense Interrupt Status

An Interrupt signal is generated by the FDC for one of the following reasons:

1. Upon entering the Result phase of:
   a. Read Data command
   b. Read A Track command
   c. Read ID command
   d. Read Deleted Data command
   e. Write Data command
   f. Format A Cylinder command
   g. Write Deleted Data command
   h. Scan commands
2. Ready Line of FDD changes state
3. End of Seek or Recalibrate command
4. During Execution phase in the non-DMA mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. During an Execution phase in non-DMA mode, DB5 in the Main Status Register is high. Upon entering the Result phase, this bit gets cleared. Reasons 1 and 4 do not require Sense Interrupt Status commands. The interrupt is cleared by Reading/Writing data to the FDC. Interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status command. This command, when issued, resets the Interrupt signal and via bits 5, 6, and 7 of Status Register 0 identifies the cause of the interrupt.

TABLE 31. INTERRUPT CAUSE

Seek End	Interrupt Code		
Bit 5	Bit 6	Bit 7	Cause
0	1	1	Ready Line changed state, either polarity
1	0	0	Normal Termination of Seek or Recalibrate command
1	1	0	Abnormal Termination of Seek or Recalibrate command

The Sense Interrupt Status command is used in conjunction with the Seek and Recalibrate commands which have no Result phase. When the disk drive has reached the desired head position, the WD37C65/A/B will set the Interrupt line true. The host CPU must then issue a Sense Interrupt Status command to determine the actual cause of the interrupt, which could be Seek End or a change in ready status from one of the drives. See Figure 7.

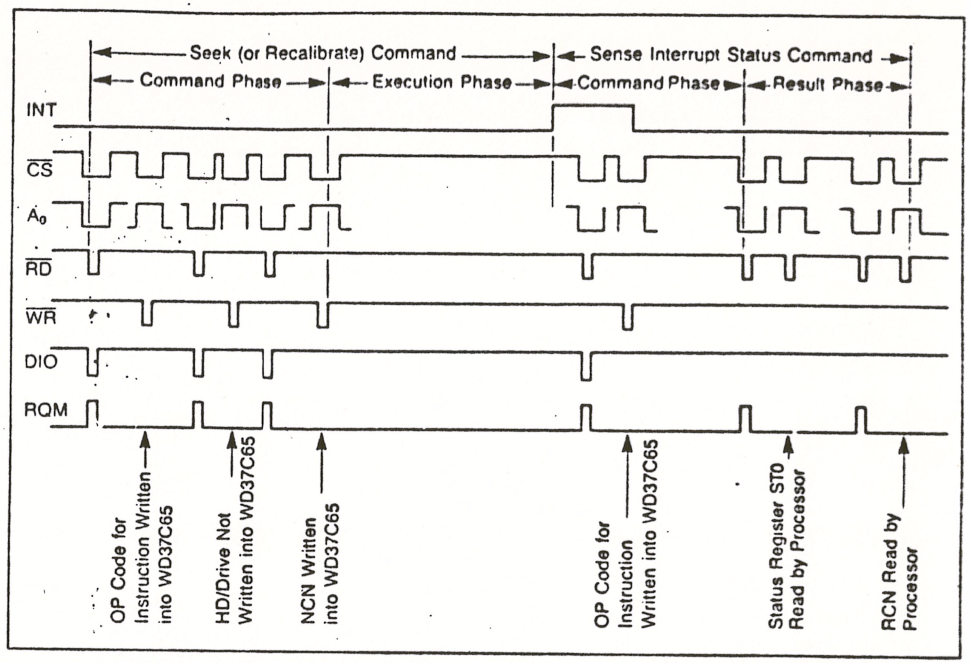

FIGURE 7. SEEK, RECALIBRATE AND SENSE INTERRUPT RELATIONSHIP

The Specify command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution phase of one of the Read/Write commands to the head unload state. This timer is programmable from 16 to 240ms in increments of 16ms (01 = 16ms, 02 = 32 ms . . . $0F_{16}$ = 240ms). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1ms, E = 2ms, D = 3ms, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and the Read/Write operation starts. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2ms, 02 = 4ms, 03 = 6ms . . . 7F = 254ms).

The time intervals mentioned above are a direct function of the clock (CLK on pin 23). Times indicated above are for a 16MHz clock; if the clock was reduced to 8MHz, then all time intervals are increased by a factor of 2.

The choice of DMA or non-DMA operation is made by the ND (Non-DMA) bit. When this bit is high (ND = 1), the Non-DMA mode is selected; and when ND = 0, the DMA mode is selected.

Sense Drive Status

This command may be used by the processor whenever it wishes to obtain the status of the FDDs. Status Register 3 contains the Drive Status information stored internally in FDC registers.

Invalid

If an Invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command after bits 7 and 6 of Status Register 0 are set to 1 and 0 respectively. No interrupt is generated during this condition. Bits 6 and 7 (DIO and RQM) in the Main Status Register are both high (1), indicating to the processor that the WD37C65/A/B is in the Result phase and the contents of Status Register 0 (ST0) must be read. When the processor reads Status Register 0, it will find an 80 hex, indicating an Invalid command was received.

A Sense Interrupt Status command must be sent after a Seek or Recalibrate interrupt; otherwise the FDC will consider the next command to be an invalid command.

In some applications, the user may wish to use this command as a No-Op command to place the FDC in a standby or No Operation state.

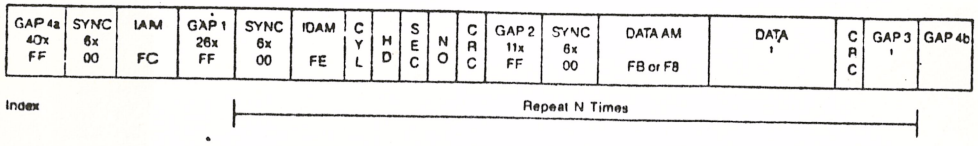

FIGURE 8. WD37C65/A/B FM MODE FORMAT

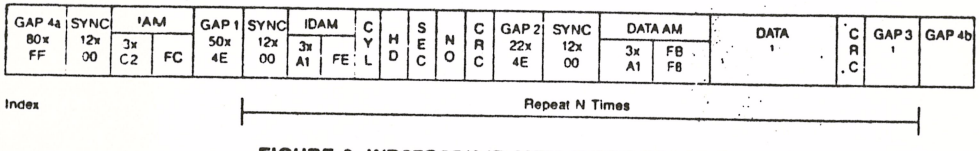

FIGURE 9. WD37C65/A/B MFM MODE FORMAT

DIFFERENCES BETWEEN NEC765 AND WD37C65/A/B

The WD37C65/A/B no longer supports certain pin functions provided for in the NEC765 predecessor. The output RW/SEEK is used in the NEC765-based subsystem as a multiplexer select line to allow a pin to have two functions depending on whether read, write, or seek type commands were under execution. This signal is no longer available externally, but is used within the WD37C65/A/B to assure that no improper pin function occurs. The LCT function has been renamed RWC and resides on a pin of its own with slightly altered active conditions and in PC AT mode is RPM/. DIRC/ is the only function on that pin and is enabled only during seeks as a power conservation measure. STEP is also only enabled during seeks and a Fault Reset (FR) is no longer needed since FLT, Fault Detects, are not sensed. FLT status, status register #3, bit 7, will always be a logic 0. Track 0, TR00/, status is only sensed during seeks as well. TS, two-sided, drive status is no longer supported, and status register #3, bits 6 and 3 will both now reflect Write Protect status. Since RDY (ready) status has no input, the WD37C65/A/B device assumes the drive is always ready. Note, this will still result in an IRQ at reset since Reset clears the status registers, then senses that RDY is true. This action is acknowledged as a change in status, and demands a Sense Interrupt Status command execution in order to clear the IRQ. Also note that the signals MFM, RDW, WCK, and VCO are no longer necessary since all logic associated with these is wholly contained within the WD37C65/A/B.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	0°C (32°F) to 70°C (158°F)
Storage Temperature	−55°C (−67°F) to +125°C (257°F)
Voltage on any pin with respect to ground	−0.3V to VCC +0.3V
Supply Voltage with respect to ground	7V

NOTE

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Operating Characteristics.

DC Operating Characteristics
TA = 0°C (32°F) to 70°C (158°F); VCC = +5V ± 10%

SYMBOL	PARAMETER	MIN	MAX	UNITS
VCC	+5VDC Power Supply	4.5	5.5	V
VIL	Input Low Voltage – Data Bus & XTOSC		0.8	V
VIH	Input High Volt – Data Bus & XTOSC	2.0		V
VILT	Input Low Threshold – Schmitt Trigger (WD37C65)	0.8	1.1	V
VILT	Input Low Threshold – Schmitt Trigger (WD37C65A/B)	0.8		V
VIHT	Input High Threshold – Schmitt Trigger(WD37C65)	1.7	2.2	V
VIHT	Input High Threshold – Schmitt Trigger (WD37C65A/B)		2.0	V
VHYS	Schmitt Trigger Hysterisis (WD37C65A/B Only)	0.45		V
VOL	Output Low - DBx,IRQ,DMA,; Io = 12.0mA		0.4	V
VOH	Output High - DBx,IRQ,DMA,; Io = −5.0mA	2.8		V
VOLHC	Output Low - High Current; Io = 48.0mA		0.4	V
ILUL	Latch Up Current Low	40.0		mA
ILUH	Latch Up Current High	−40.0		mA
ILL	Leakage Current Low (WD37C65)		10.0	uA
ILLX	Leakage Current Low (WD37C65A/B Only)		20.0	uA
ILH	Leakage Current High (WD37C65)		−10.0	uA
ILHX	Leakage Current High (WD37C65A/B Only)		−20.0	uA
ICC	Supply Current – 100uA Source Loads (WD37C65)		35.0	mA
ICC	Supply Current – 100uA Source Loads (WD37C65A/B)		45.0	mA
ICCHL	Supply Current – 5.0mA Source Loads (WD37C65)		85.0	mA
ICCHL	Supply Current – 5.0mA Source Loads (WD37C65A/B)		95.0	mA
PD	Power Dissipation – ICC Max * (WD37C65)		375.0	mW
PD	Power Dissipation – ICC Max * (WD37C65A/B)		425.0	mW
PDHL	Power Dissipation – ICCHL Max * (WD37C65)		525.0	mW
PDHL	Power Dissipation – ICCHL Max * (WD37C65A/B)		575.0	mW
VPQR	Power Qualified Reset Threshold (WD37C65A/B Only)	2.8	4.35	V

* Includes open drain high current drivers at Vol = 0.4V.

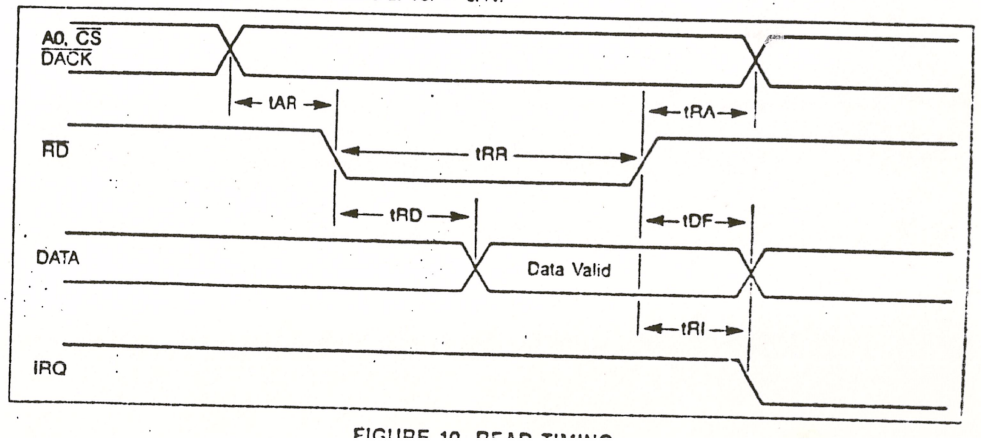

FIGURE 10. READ TIMING

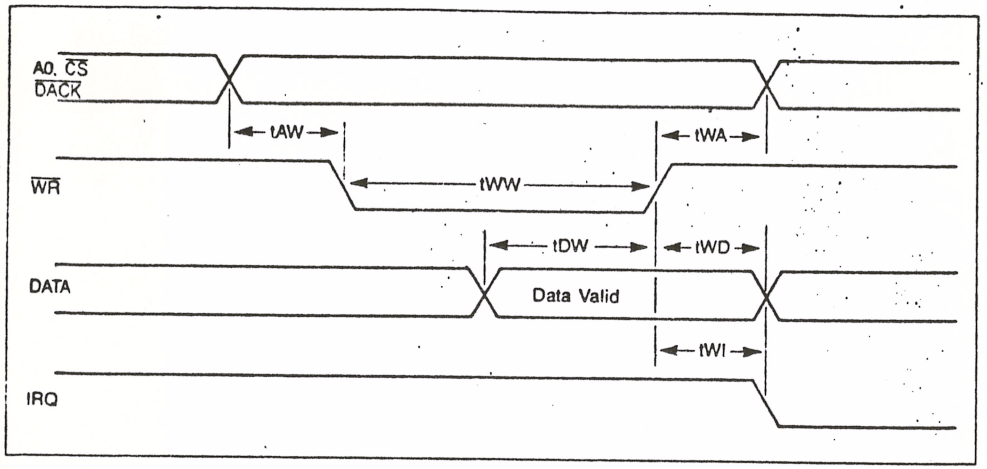

FIGURE 11. WRITE TIMING

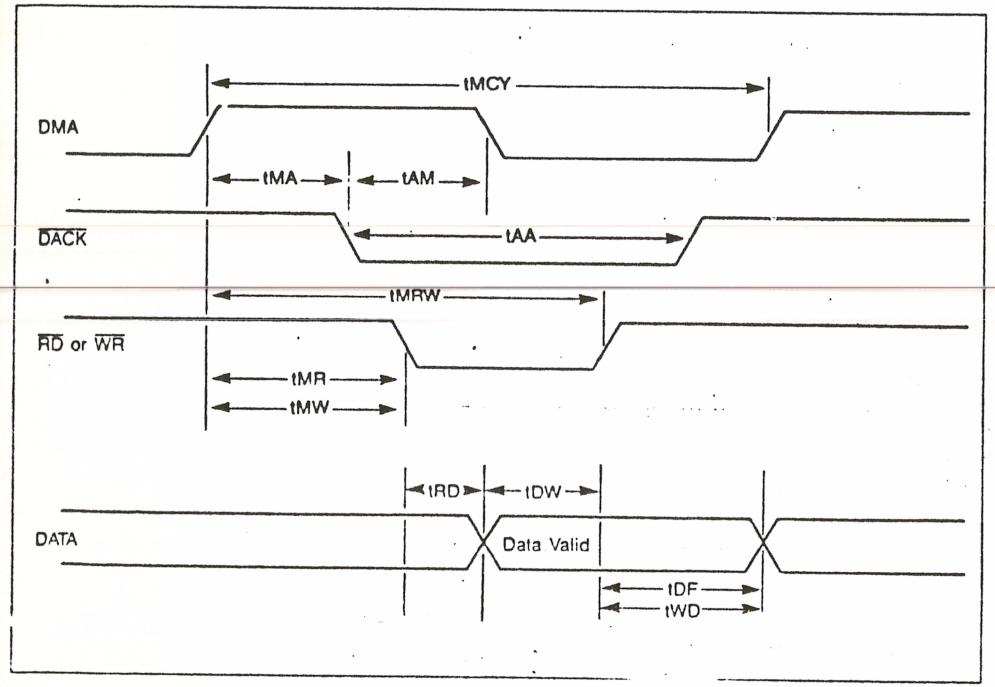

FIGURE 12. DMA TIMING

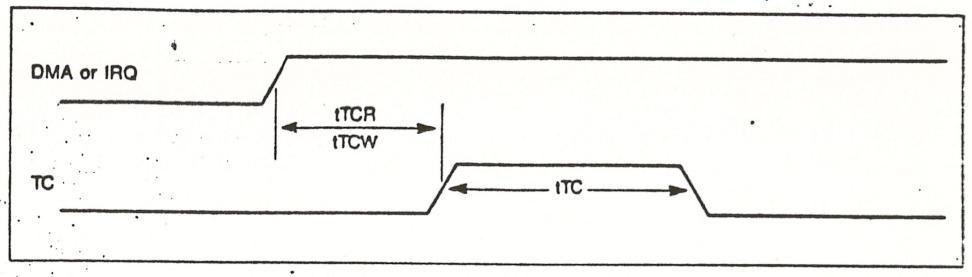

FIGURE 13. TERMINAL COUNT TIMING

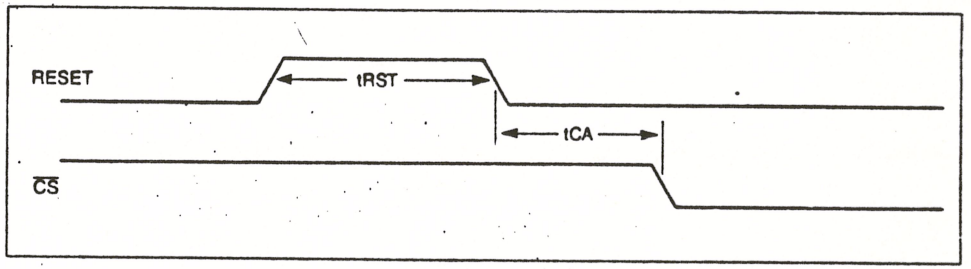

FIGURE 14. RESET TIMING

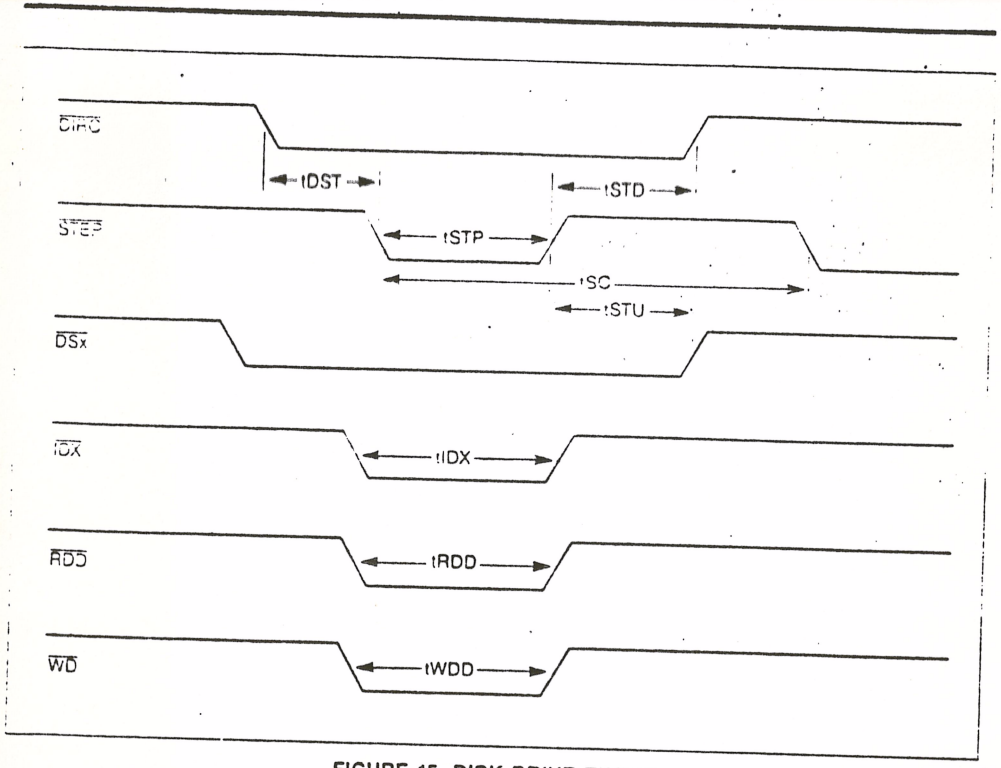

FIGURE 15. DISK DRIVE TIMING

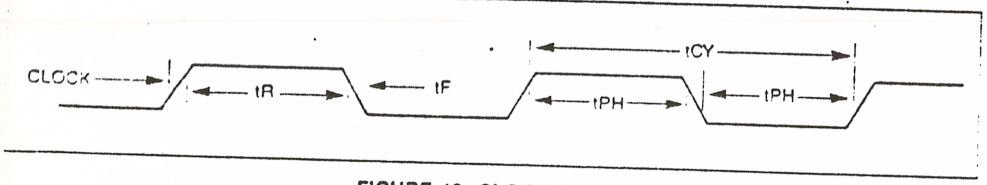

FIGURE 16. CLOCK TIMING

AC Operating Characteristics
TA = 0°C (32°F) to 70°C (158°F); VCC = +5V ± 10%
CL = 100pf

SYMBOL	PARAMETER	MIN	MAX	UNITS
tCY	Clock Period	60		nS
tPH	Clock Active (High or Low)	25		nS
tR	Clock Rise Time (Vin 0.8 to 2.0)		5	nS
tF	Clock Fall Time (Vin 2.0 to 0.8)		5	nS
tAR	A0,CS,DACK Set Up Time to RD Low	0		nS
tRA	A0,CS,DACK Hold Time to RD High	0		nS
tRR	RD Width	90		nS
tRD	Data Access Time From RD Low		90	nS
tDF	DB To Float Delay From RD High	10	65	nS
tAW	A0,CS,DACK,LDCR,LDOR, Set Up Time To WR Low	0		nS
tWA	A0,CS,DACK,LDCR,LDOR, Hold Time From WR High	0		nS
tWW	WR Width	60		nS
tDW	Data Set Up Time To WR High	80		nS
tWD	Data Hold Time From WR High	0		nS
tRI	IRQ Reset Delay Time From RD High		1MCY +150nS	
tWI	IRQ Reset Delay Time From WR High		1MCY +150nS	
tMCY	DMA Cycle Time	52		MCY
tAM	DMA Reset Delay Time From DACK Low		140	nS
tMA	DACK Delay Time From DMA High	0		nS
tAA	DACK Width	90		nS
tTC	TC Width	60		nS
tRST	Reset Width – TTL Driven CLK1	250		nS
tSRST	Reset Width – Software Reset	5		MCY
tRDD	RDD Active Time Low	40		nS
tWDD	WD Write Data Width Low	1/2 (TYP)		WCY
tDST	DIRC Hold & Set Up To STEP Low	4		MCY
tSTU	DSX Hold Time From STEP Low	20		MCY
tSTP	STEP Active Time Low	24		MCY
tSC	STEP Cycle Time	132		MCY
tSTD	DIRC Hold Time After STEP	96		MCY
tIDX	IDX Index Pulse Width	2		MCY
tMR	RD Delay From DMA	0		nS
tMW	WR Delay From DMA	0		nS
tMRW	RD Or WR Response From DMA High		48	MCY
tCA	Chip Access Delay From RST Low – TTL	32		MCY
tCAS	Chip Access Delay From tSRST Low	40		MCY
tXCA	Chip Access Delay from RST – OSC XT1 At 16 MHz	500		uS
tXTS	XT2 Access Delay After RST 9.6 MHz	1000		uS
tTCR	TC Delay From Last DMA Or IRQ, RD	0	192	MCY
tTCW	TC Delay From Last DMA Or IRQ, WR	0	384	MCY

CY specifies CLK1 or XT1 period
MCY specifies MCLK period, dependent on selected data rate
WCY specifies WCLK period, dependent on selected data rate