

THOMSON-EFCIS

Integrated Circuits

ADVANCE INFORMATION

SINGLE CHIP ASYNCHRONOUS FSK MODEM

The EFB7512 is a single chip asynchronous Frequency Shift Keying (FSK) voiceband modem.

Operating at rates up to 75, 1200 bits per second, it is compatible with the applicable CCITT recommended standards for V23 type modems.

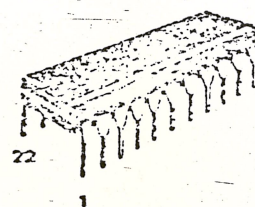
This device provides the essential CCITT V24, V25 and V54 terminal control signals at TTL levels.

- Monolithic device includes both transmit and receive filters
- Standard low cost crystal (3.579 MHz)
- $\pm 5\%$ power supplies (+5 V, -5 V)
- Separate analog and digital ground pins reduce system noise problems
- Receive and transmit clocks for UART, 19200 Hz clock available.
- Reference voltage internally generated, to avoid noise and supply drift
- Programmable modes:
75 bds transmission/1200 bds reception,
1200 bds transmission/75 bds reception, 2 wire operations
or 1200 bds transmission/1200 bds reception 4 wire F.D. operations.
- Fixed compromise line equalizer
- Low power consumption : 100 mW typical
- Direct interface to the THOMSON-EFCIS EF6850 UART.

EFB7512

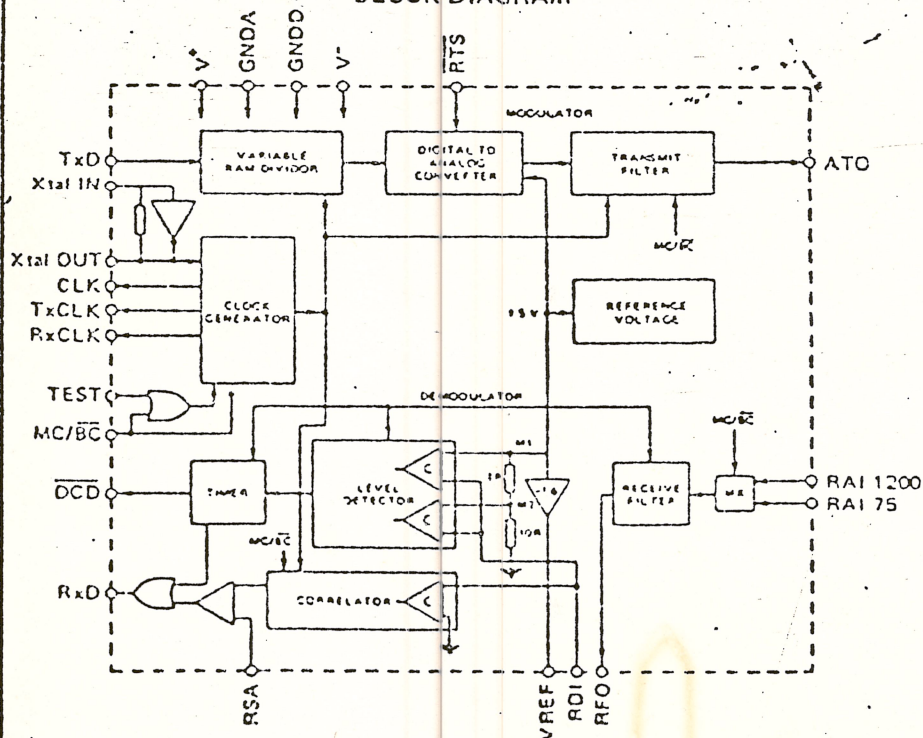
SINGLE CHIP
ASYNCHRONOUS
FSK MODEM

CASE CB-180



P SUFFIX
PLASTIC PACKAGE

BLOCK DIAGRAM



PIN ASSIGNMENT

TEST	1	22	MC/BC
RTS	2	21	TxD
GND	3	20	CLK
V+	4	19	RxCLK
RFO	5	18	TxCLK
ATO	6	17	Xtal IN
V-	7	16	Xtal OUT
RAI75	8	15	PDI
RAI1200	9	14	DCD
GND	10	13	RxD
RSA	11	12	VREF

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THOMSON
CORPORATION

EFB7512

ABSOLUTE MAXIMUM RATINGS *

Rating	Symbol	Value	Unit
Supply voltage	V^+	+7 V	V
Supply voltage	V^-	-7 V	V
Analog input range	V_{in}	$V^- \leq V_{in} \leq V^+$	V
Digital input range	V_I	$GNDD \leq V_I \leq V^+$	V
Operating temperature range	T_A	0 to 70	°C
Storage temperature range	T_{stg}	-55 to +125	°C
Pin temperature (Soldering, 10 s)		260	°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Standard CMOS handling procedures should be employed to avoid possible damage to device.

ELECTRICAL OPERATING CHARACTERISTICS

Parameter	Symbol	Min	Nominal	Max	Unit
Positive Supply Voltage	V^+	4.75	5.0	5.25	V
Negative Supply Voltage	V^-	-5.25	-5.0	-4.75	V
V^+ Operating current	I_{CC}	—	—	15	mA
V^- Operating current	I_{BB}	-10	—	—	mA

D.C. AND OPERATING CHARACTERISTICS

($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V^+ = +5\text{ V} \pm 5\%$, $V^- = -5\text{ V} \pm 5\%$, $GNDA = 0\text{ V}$, $GNDD = 0\text{ V}$, unless otherwise noted).

DIGITAL INTERFACE (TEST, $\overline{RTS}$, $\overline{DCD}$, RxD , $TxCLK$, $RxCLK$, CLK , TxD , $MC/\overline{BC}$)

Parameter	Symbol	Min	Typ (1)	Max	Unit
Input Current ($V_{IL\text{ min}} \leq V_I \leq V_{IH\text{ max}}$)	I_I	—	—	1	mA
Output low level current ($V_{OL} = 0.4\text{ V}$)	I_{OL}	1.6	—	—	mA
Output high level current ($V_{OH} = 2.8\text{ V}$)	I_{OH}	—	—	-250	μA
Input low voltage	V_{IL}	$GNDD$	—	0.8	V
Input high voltage	V_{IH}	2.4	—	V^+	V

Note : 1 — Typical values are for $T_A = 25^\circ\text{C}$ and nominal power supply values.

D.C. AND OPERATING CHARACTERISTICS (continued)

(T_A = 0°C to +70°C, V⁺ = +5 V ± 5%, V⁻ = 5 V ± 5%, GNDA = 0 V, GNDD = 0 V, unless otherwise specified)

ANALOG INTERFACE, RECEIVE FILTER (RAI 75, RAI 1200, RFO)

Parameter	Symbol	Min	Typ (1)	Max	Unit
Input leakage current, (-3 V < V _{IN} < 3 V)	I _{BRI}	-	±1	±3	μA
Input resistance,	R _{IRI}	1	3	-	MΩ
Output offset voltage	V _{OGSR}	-	-	±300	mV
Output voltage swing, (R _L ≥ 10 kΩ)	V _{OIRI}	-	-	±2	V
Load capacitance,	C _{LRI}	-	-	20	pF
Load resistance,	R _{LRI}	10	-	-	kΩ
Input voltage swing	V _{IRI}	-3	-	+3	V
Signal frequency distortion products at maximum signal level	CDPR	-	-40	-	dB

ANALOG INTERFACE RECEIVE DEMODULATOR INPUT (RDI)

Parameter	Symbol	Min	Typ (1)	Max	Unit
Input current	I _{in}	-1	-	1	μA
Maximum detection level to valid DCD output	N ₁	1.1	1.3	1.5	V
Minimum detection level to valid DCD output	N ₂	-	0.73	-	V
Hysteresis effect	N1/N2	-	1.8	-	
		4	5	6	dB

ANALOG INTERFACE, RECEIVE SLICER ADJUST (RSA)

Parameter	Symbol	Min	Typ	Max	Unit
Input current	I _{in}	-1	-	+1	μA
Input voltage	V _I	V _{REF}	V _{REF} /2	GNDA	V

ANALOG INTERFACE, TRANSMIT OUTPUT (ATO)

Parameter	Symbol	Min	Typ (1)	Max	Unit
Output DC offset, (RTS connected to V ⁺)	V _{OS}	-	-	±250	mV
Load capacitance	C _L	-	-	20	pF
Load resistance	R _L	10	-	-	kΩ
Output voltage swing (R _L = 10 kΩ, C _L = 20 pF)	V _O	2.8	3	3.2	V _{pp}
	-	0	0.5	1	dB
	V _O	2.8	3	3.2	V _{pp}
	-	0	0.5	1	dB
RTS attenuation ratio efficiency	-	55	-	-	dB

(1) Typical values for T_A = 25°C and nominal power supply values.

ANALOG INTERFACE, REGULATED VOLTAGE (V_{REF})

Parameter	Symbol	Min	Typ (1)	Max	Unit
Output voltage	V_{OR}	-2.5	-2	-1.5	V
Load resistance	R_{LR}	10	—	—	$k\Omega$
Load capacitance	C_{LR}	—	—	20	pF

(1) Typical values for $T_A = 25^\circ\text{C}$ and nominal power supplies values.

DYNAMIC CHARACTERISTICS

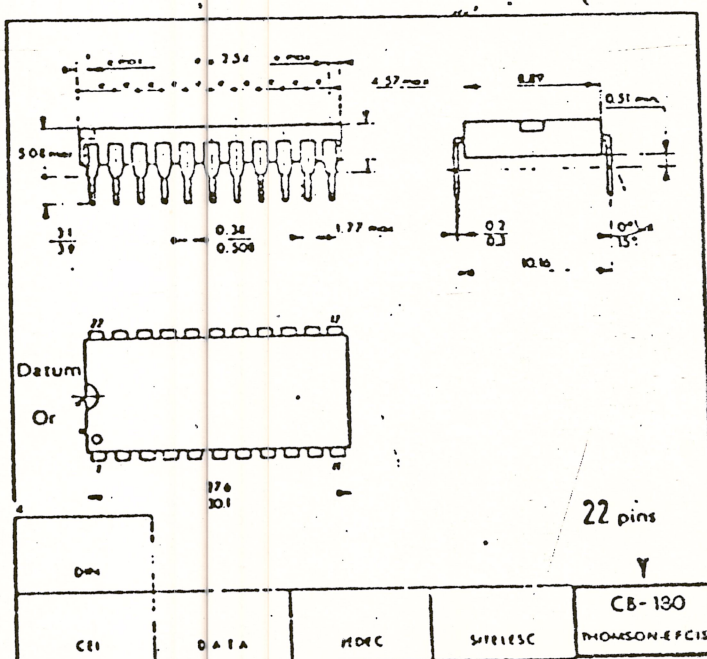
RECEIVE FILTER TRANSFER CHARACTERISTICS

Parameter			Symbol	Min	Typ	Max	Unit
Absolute passband gain at 525 or 2100 Hz (V_{RFO} , $R_L = \infty$)			GAR	-3.2	-2.9	-2.6	dB
Gain relative to gain at 525 or 2100 Hz Maximum input signal	2100 Hz	525 Hz					
	380 Hz	95 Hz	GRR	-	-65	-55	dB
	460 Hz	115 Hz	"	-	-65	-55	dB
	1100 Hz	275 Hz	"	-4.7	-4.4	-4.1	dB
	2800 Hz	700 Hz	"	-23	-20	-17	dB
	10000 Hz	2500 Hz	"	-10	-8.5	-7	dB

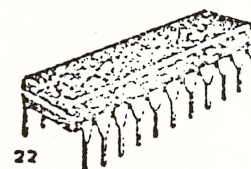
DIGITAL INTERFACE

Parameter	Symbol	Min	Typ	Max	Unit
Capacitance	C_{IB}	—	—	10	pF
Input rise-time, fall-time, measured between 0.8 V and 2.4 V	t_{THL} , t_{TLH}	—	—	100	ns
Output rise-time, fall time between 0.4 V and 2.8 V (1)	t_{THL} , t_{TLH}	—	50	—	ns

(1) Driving one 74L or 74LS TTL load plus 30 pF.



CASE CB-180

P SUFFIX
PLASTIC PACKAGE

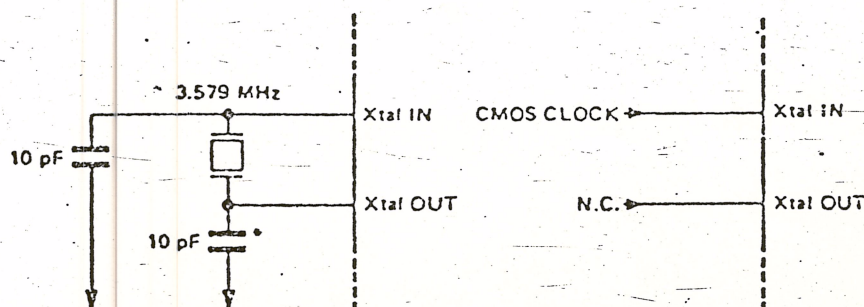
RECEIVE SECTION

TEST	1	Loop back mode	When this input is high, the demodulator is tuned on the transmission modulation rate to the loop back mode or to the 4 wires full duplex operation mode. When TEST is low, the modem is in normal operating mode.
RFO	5	Receive filter output	This analog output must be connected to a high-pass filter and slicer, with sufficient gain to satisfy the level detection conditions.
RAI 75	8	Receive analog input	(75 bds line signal reception). Input for 75 bds modulated analog signal of an amplitude lower than 6 V peak to peak and centered on analog ground.
RAI 1200	9	Receive analog input	(1200 bds line signal reception). Input for 1200 bds modulated analog signal of amplitude lower than 6 V peak to peak and centered on analog ground.
RDI	15	Receive demodulator input	This is the input of the demodulator. The analog signals are passed through level detection comparators and zero crossing detector.
RSA	11	Receive slicer adjust	Input of the decision comparator optimizing discrimination between high and low frequencies.
DCD	14	Data carrier detect	This output is low when the EFB7512 receives on input RDI a signal with amplitude higher than N1. This output is high when the EFB7512 receives on input RDI a sinusoidal signal with amplitude lower than N2. Within the N1 — N2 range, the detection system presents an hysteresis.
RxD	13	Receive data	This output is low when a high frequency signal is present on input RDI, and high when a low frequency signal is present on input RDI. Without CARRIER on pins RAI, this output is high.
RxCLK	19	Receive clock	This output delivers a clock signal, the frequency of which is 16 times of the demodulation rate. ($\pm 1\%$) The logic state duration is compatible to the UART clock specification.

FUNCTIONAL DESCRIPTION

CLOCK GENERATION

Crystal :
NYMPH, NYP 035A-18



* Capacitor values vary with different crystal manufacturers

With a minimum number of external components, the EFB7512 performs all the functions of modulation, demodulation and filtering necessary to meet the requirements of CCITT Recommendation V.23 and BELL Standard 202.

This circuit is in four parts :

- a modulator,
- a demodulator,
- a clock generator,
- a reference voltage generator.

Note : The description of the demodulator also covers a subsystem, external to the circuit proper and having the following functions (refer to typical application annex):

- high-pass filter,
- amplification,
- slicer.

MODULATOR

When input RTS is low, output ATO delivers a sinusoidal signal, the frequency of which depends on MC/BC and TxD.

DEMODULATOR

An analog multiplexer selects RAI 75 input or RAI 1200 input according to the demodulation rate selected by the MC/BC and TEST inputs (refer to demodulator functional characteristics).

When the analog signal on RDI conforms to certain criteria, output DCD detects it and output RxD delivers a digital signal, the logic state of which depends on the analog signal frequency.

CLOCK GENERATOR

This part of the circuit generates from a 3.579 MHz crystal all the internal clocks necessary to the correct performance of the EFB7512 : ie clocks for the switched capacitor filters as well as those for the sinewave generator. The circuit also delivers on RxCLK and TxCLK, the transmit and receive clocks for the UART.

REFERENCE VOLTAGE GENERATOR

This part of the circuit generates a regulated voltage on VREF which is used to adjust detection thresholds. It is independent of power supply values.

FUNCTIONAL CHARACTERISTICS

MODULATOR

- Modulation conditions:

RTS	ATO
"L"	FSK modulated signal
"H"	GNDA

- Transmitted frequencies :
(for details of frequency selection see PIN DESCRIPTION - ATO)

MC/ $\overline{BC}$	Modulation rate	TxD	R.35 and V.23 Recommendations (Hz)	Frequency generated from a 3.579 MHz crystal	Error (Hz)
GNDD	75 bauds	"H"	390 ± 2	389.52	-0.48
		"L"	450 ± 2	450.20	+0.20
V*	1 200 bauds	"H"	$1\,300 \pm 10$	1 299.70	-0.34
		"L"	$2\,100 \pm 10$	2 097.40	-2.61

DEMODULATOR

- Frequencies received on RDI

Analog signals centered on analog ground are received on input RDI.

RECEIVE DEMODULATION RATE

The receive demodulation rate depends on MC/ $\overline{BC}$ and TEST inputs as follows :

MC/ $\overline{BC}$	TEST	DEMODULATION RATE	FREQUENCIES (recommendation V23)
H	H	1200	1300 ± 16 2100 ± 16
L	H	75	390 450
H	L	75	390 450
L	L	1200	1300 ± 16 2100 ± 16

- Level detection conditions

Input RDI drives a signal detector the output of which ($\overline{DCD}$) is at logic "0" if the level of signal RDI is higher than N1. The output of this detector is at logic "1" if the level of signal RDI is lower than N2. This detector has a hysteresis effect : N1/N2.

- Timing detection conditions

The timing performance of the level detector ($\overline{DCD}$) conforms to CCITT Recommendation V.24.

Under normal working conditions, output $\overline{DCD}$ is :

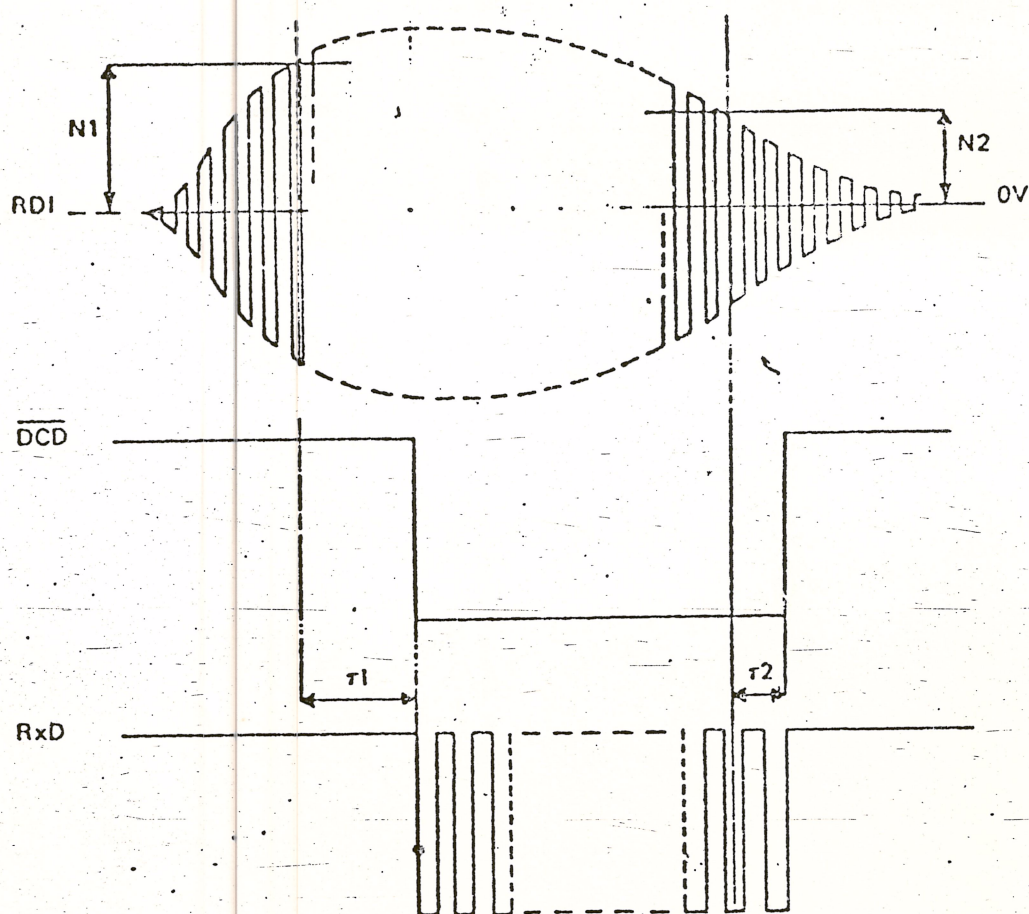
- low if signal RDI conforms to the level detection condition,
- high if signal RDI does not conform to the level detection conditions.

Output $\overline{DCD}$ goes from high to low when signal RDI conforms to the level detection conditions for 20 ms or more (respectively 80 ms for 75 bauds).

Output $\overline{DCD}$ does not go from high to low when signal RDI conforms to the level detection conditions for 10 ms or less (respectively 0 for 75 bauds).

Output $\overline{DCD}$ goes from low to high when signal RDI does not conform to the level detection conditions for 15 ms or more (respectively 80 ms for 75 bauds).

Output $\overline{DCD}$ does not go from low to high when signal RDI does not conform to the level detection conditions for 5 ms or less (respectively 15 ms for 75 bauds).



Modulation rate	DCD transition	Min	Typ (1)	Max	Unit
1200 bds	τ_1	10	13	20	ms
	τ_2	5	13	15	ms
75 bds	τ_1	0	43	80	ms
	τ_2	15	43	80	ms

(1) Typical values for $T_A = 25^\circ\text{C}$ and nominal power supply values.

• Demodulated signal

Under normal working conditions, signal RxD conforms to the following table :

Demodulation rate	Level received on RDI	DCD	Frequency received on RAI (Hz)		RxD
			RAI 75	RAI 1200	
1200 bds	$> N1$	"L"	"X"	1300	"H"
	$> N1$	"L"	"X"	2100	"L"
	$< N2$	"H"	"X"	"X"	"H"
75 bds	$> N1$	"L"	390	"X"	"H"
	$> N1$	"L"	450	"X"	"L"
	$< N2$	"H"	"X"	"X"	"H"

• REFERENCE VOLTAGE GENERATOR

The VREF output carries a regulated reference voltage.

An external potentiometer, connected between VREF and GNDA, can supply a regulated voltage to input RSA.

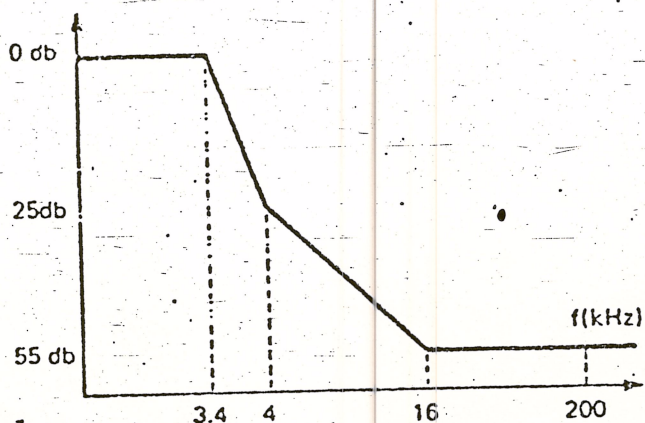
Adjustment of RSA optimizes the discrimination between the high and low frequencies.

TYPICAL PERFORMANCES

These typical performances are achieved with the environment described further. (See Annex II).

• Transmitted spectrum

On output ATO, the transmitted signal energy outside the voiceband related to the 300, 3400 Hz transmitted signal energy must conform to the following specification:



• Receiver

Measurement conditions

Local transmit level : -2 dBm on 75 baud back channel.
Receive level : -25 dBm, with 511 bit pseudo-random test pattern.

Isochronous distortion

Table below shows the typical isochronous distortion values obtained with the EFB7512, which conform to the CCETT specifications for videotex applications. The characteristics of CCETT lines used for measurements are given in Annex I.

LINE	1200 RECEPTION	75 RECEPTION
Line 1 (flat)	10 %	5 %
Line 2	14 %	6 %
Line 3	14 %	14 %
Line 4	12 %	6 %

Bit error rate

The typical bit error rates versus white noise are as follows.

	1200 bds reception		75 bds reception	
	S/N	BER	S/N	BER
on line 1	6 dB	$2 \cdot 10^{-3}$	4 dB	10^{-3}
on line 2	7 dB	$3 \cdot 10^{-4}$	4 dB	10^{-3}
on line 3	9 dB	$2 \cdot 10^{-4}$	4 dB	10^{-3}
on line 4	8 dB	$2 \cdot 10^{-4}$	4 dB	10^{-3}

ENVIRONMENTAL FUNCTIONAL DESCRIPTION

(See diagram shown next page)

Transmit section (A4)

The transmit section comprises a single operational amplifier capable of driving a load of 600 Ω , which can also be used to adjust the transmit level.

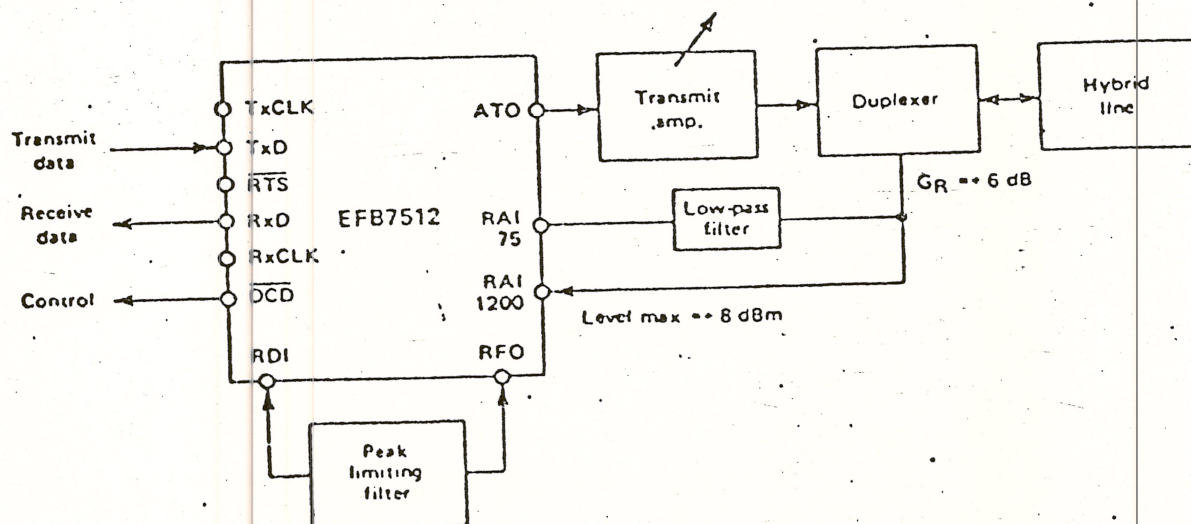
Duplexer (A1)

This amplifier provides the 2 wire/4 wire separation function and enables a low cost standard non differential transformer (ratio 1:1) to be used. The duplexer principle provides a gain of 6 dB for the received signal.

Peak-limiting filter

This section is made of two operational amplifiers and performs three functions :

- peak-limiting amplifier, designed to meet the signal detector levels according to the signal received from the phone line.
- High-pass filter (12 dB per octave) to overcome the DC component of the signal to be demodulated.
- Low-pass filter to protect against the inherent noise of the receive filter.



CALCULATION OF CIRCUIT ELEMENTS

The following factors must be considered in calculating the external components in the EFB7512 application :

- Signal attenuation introduced by the receive filter is 3 dB.

- The maximum permissible level at RAI 1200 input is 6 Vpp (± 8 dBm).

Note : the reference frequency is 2100 Hz.

- A 5 dB hysteresis is introduced within the two signal detection level N1 and N2, in accordance with CCITT Recommendation V.23.

To be centered, the two limit values of the CARRIER DETECT signal are therefore :

- Upper : -43 dBm, or 15.5 mVpp
- Lower : -48 dBm, or 8.7 mVpp

- For a correct operation of the EFB7512 signal detector, the peak-limiting filter must remain linear up to -43 dBm on line.

- At input RDI, the upper threshold level N1 of the signal detector is 2.6 Vpp (1.5 dBm), and must correspond to the minimum signal level received from the line transformer. With a duplexer reception gain of $+6$ dB, the peak-limiting filter gain is defined by :

$$A = 43 - 6 + 3 + 1.5 = 41.5 \text{ dB (a ratio of 119)}.$$

- The signal attenuation introduced by the 75 dBs receive filter is -3.5 dB. The maximum level on RAI 75 is 6 Vpp (± 8 dBm). An additional external filtering is necessary in order to suppress 1200 bds modulation spurious signal which are not eliminated by the duplexor. The attenuation of this additional filtering must be between -5 dB and $+1.5$ dB in order to achieve DCD characteristics at 450 Hz equivalent to main channel. The following typical application of the EFB7512 conforms to the above conditions.

Note : The peak-limiting filter gain must be adjusted according to the minimum level on line. With a minimum level of :

$$-38 \text{ dBm, } A = 36.5 \text{ dB}$$

$$-33 \text{ dBm, } A = 31.5 \text{ dB}.$$

ANNEX I

