DACK								MA				REG	END (HEX)
0	1	2	3	4	5	6	7	3	2	1	0		
0	1	1	1	0	1	1	1	0	1	1	1	7	087
1	0	1	1	0	1	1	1	0	0	1	1	3	083
1	1	0	1	0	1	1	1	0	0	0	1	1	081
1	1	1	0	0	1	1	1	0	0	1	0	2	082
1	1	1	1	1	0	1	1	1	0	1	1	B	08B
1	1	1	1	1	1	0	1	1	0	0	1	9	089
1	1	1	1	1	1	1	0	1	0	1	0	A	08A
1	1	1	1	1	1	1	1	1	1	1	1	F	08F

DACK 4 → INDICA SE O CANAL ATIVO PERTENCE AO DMA 1 OU DMA 2

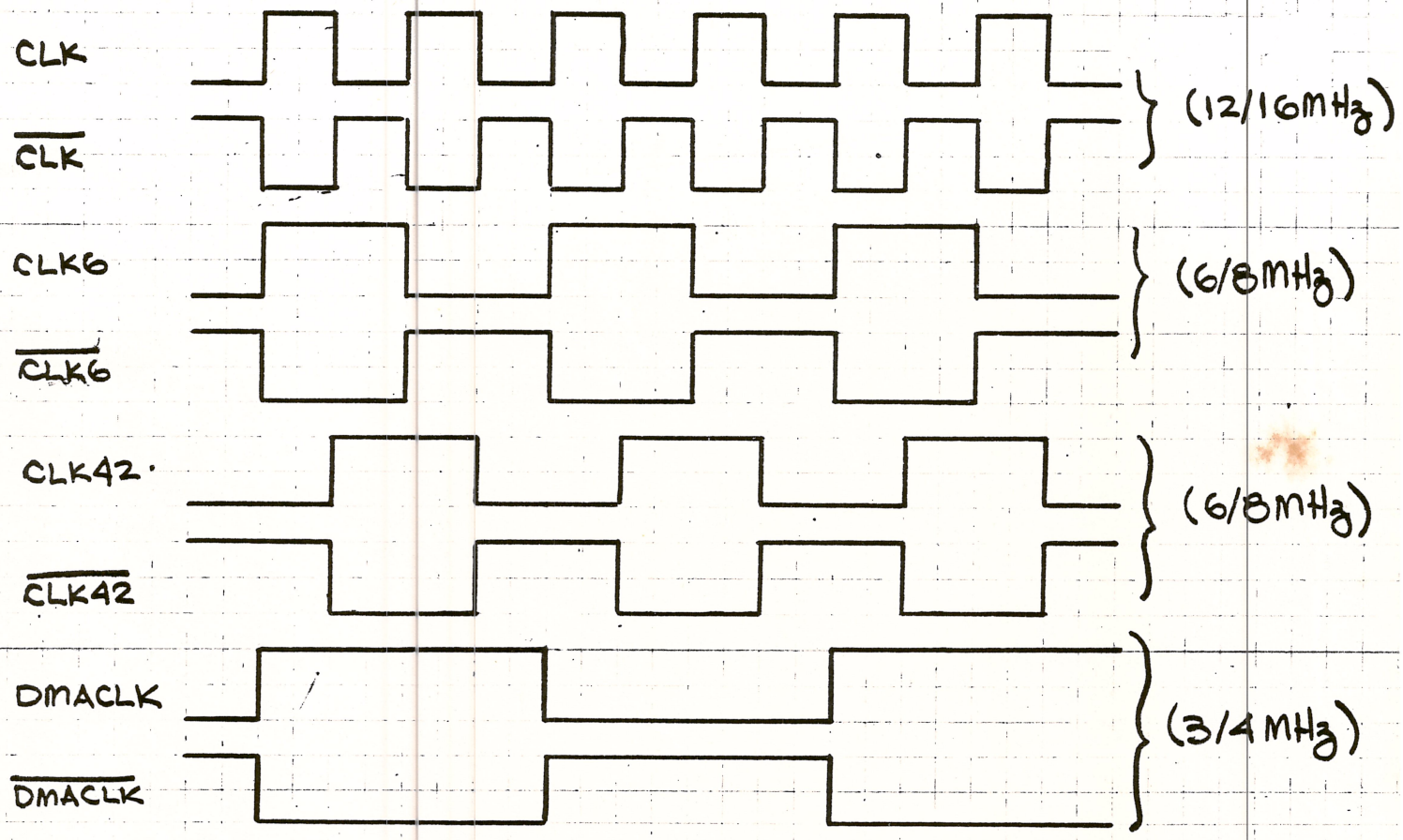
DMACLK → 3MHz → 333 ns → ×5 → 1,66 µs

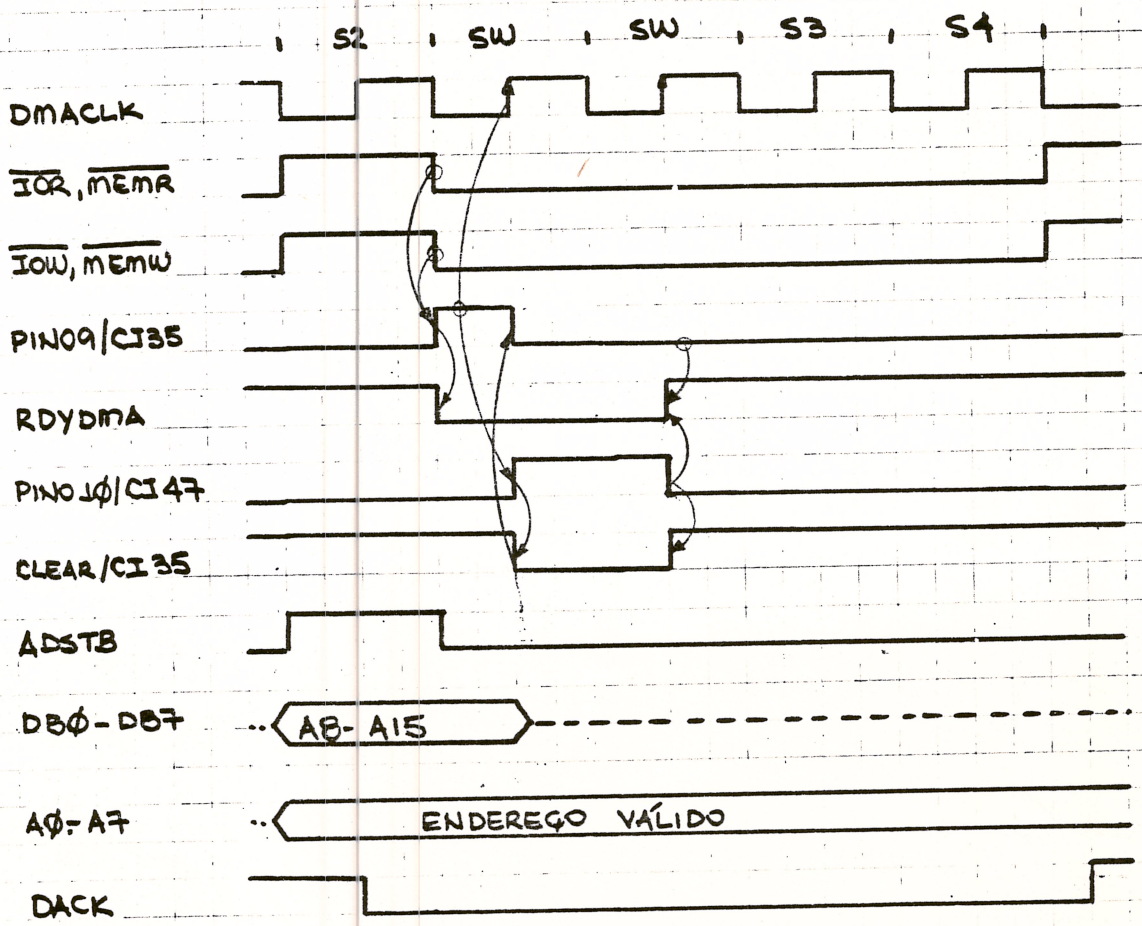
4MHz → 250 ns → 1,25 µs

CPU (1wait) → (tramf. 8→8) → (6MHz) 1 µs — (8MHz) 750 ns

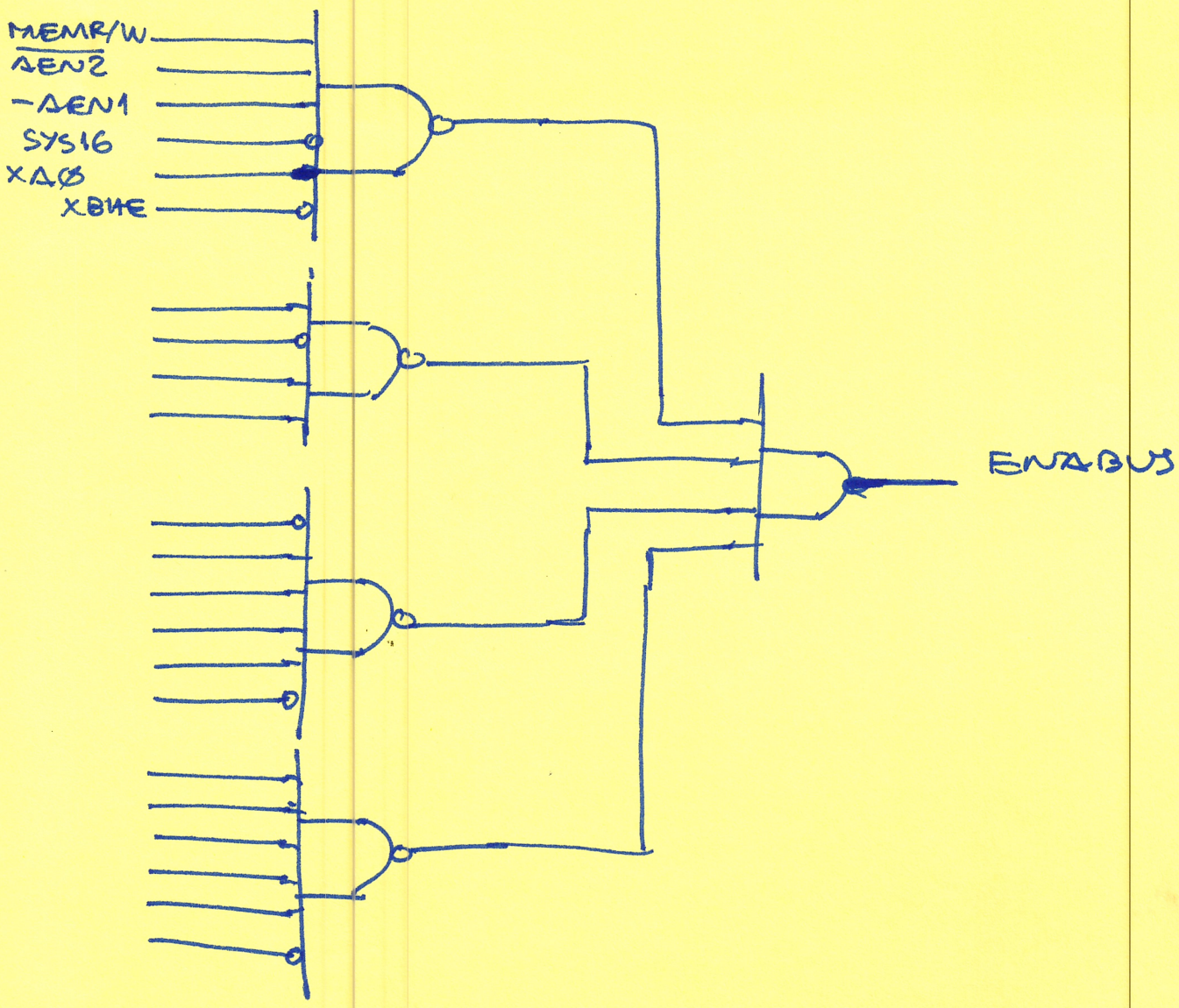
1Owait → tramf. 16→8 → 2 µs — 1,5 µs

1wait → " 16→16 → 500ns — 375ns.
8→16

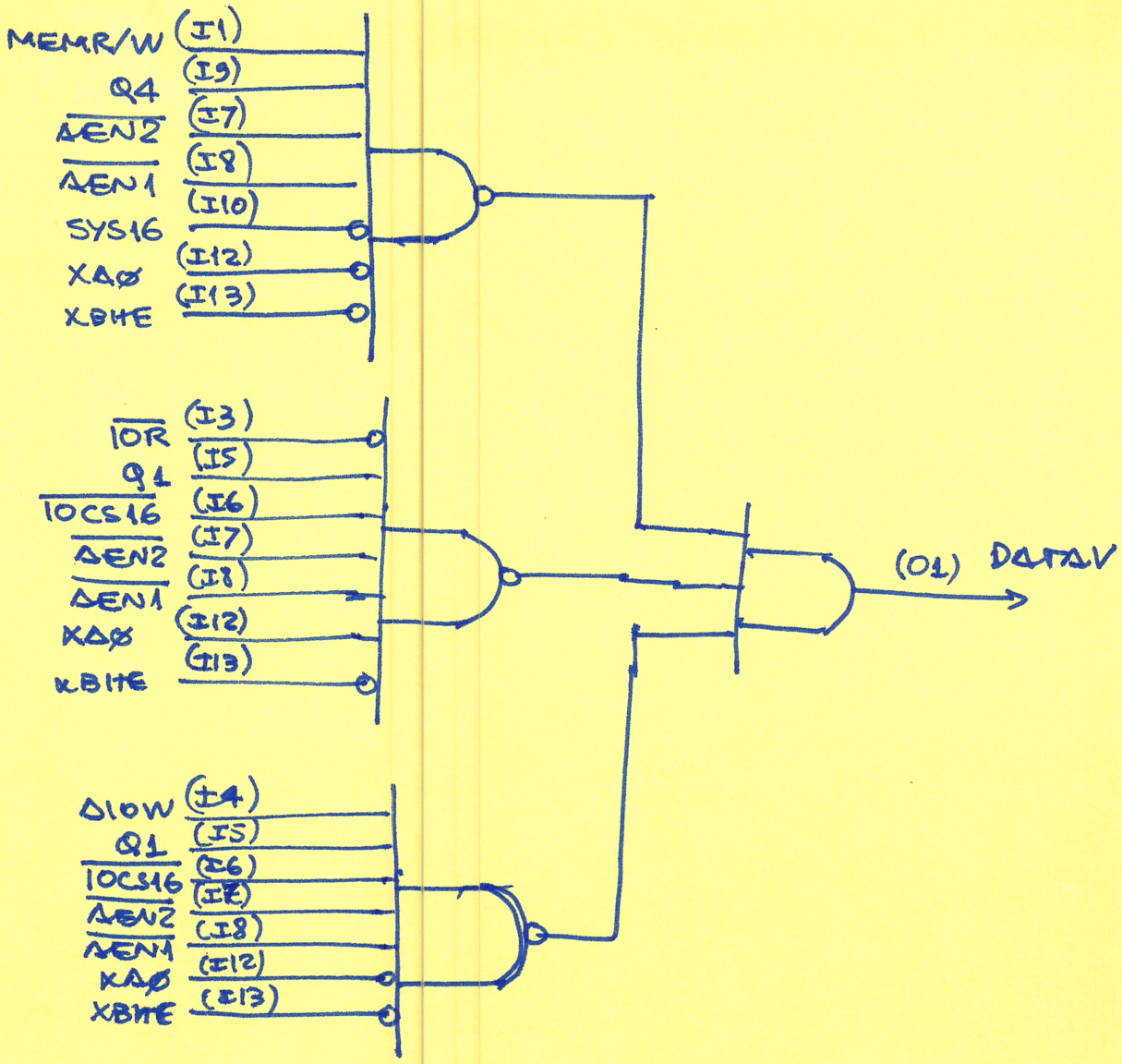

CLK
$\overline{CLK}$
(12/16MHz)
CLK6
$\overline{CLK6}$
(6/8MHz)
CLK42
$\overline{CLK42}$
(6/8MHz)
DMACLK
$\overline{DMACLK}$
(3/4MHz)



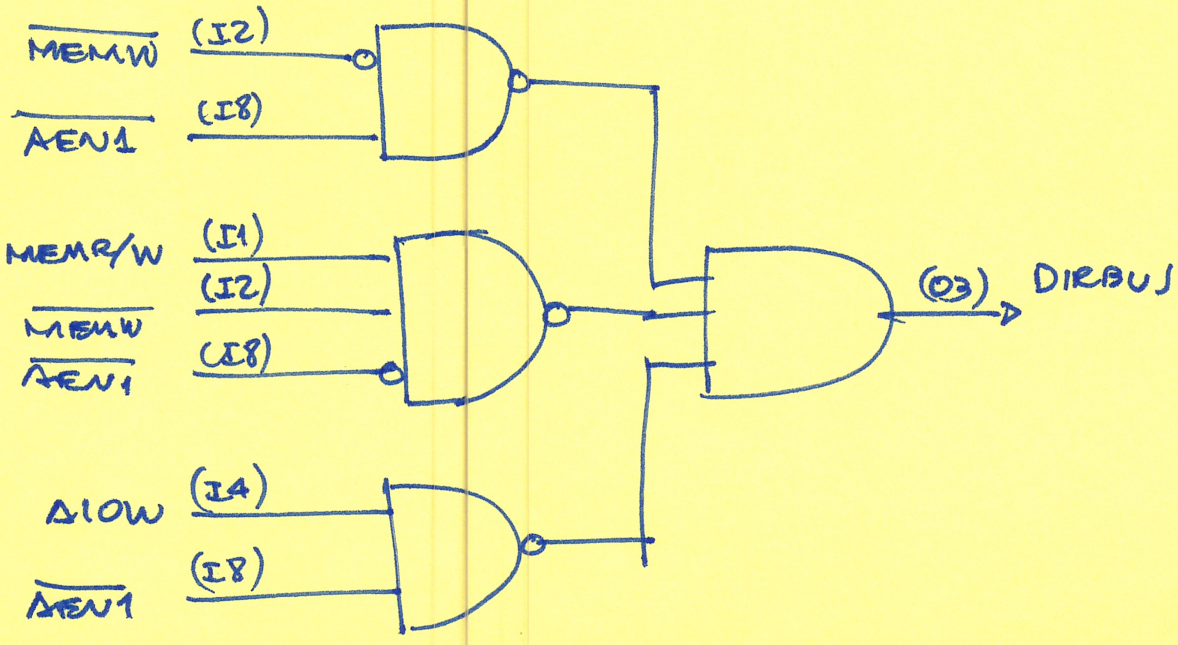
CICLO DE DMA ($\overline{DMAAEN}$ = 0)


MEMR/W
SEN2
-SEN1
SYS16
XA0
XBHE
ENABUS

PAL 16L8-A CE40 (Controle do Bus)



PAL 16L8-A- CC40 (Controle do Bus)



TOTAL ALE → TALE

VALE → VIRTUAL ALE