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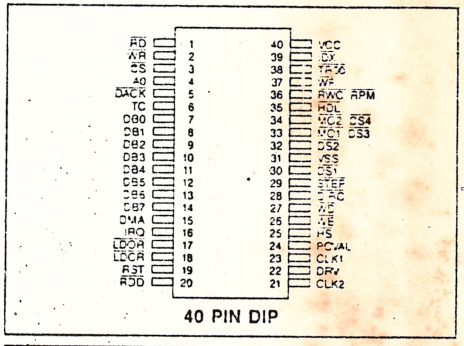
WESTERN DIGITAL

WD1002S 5 88 7M

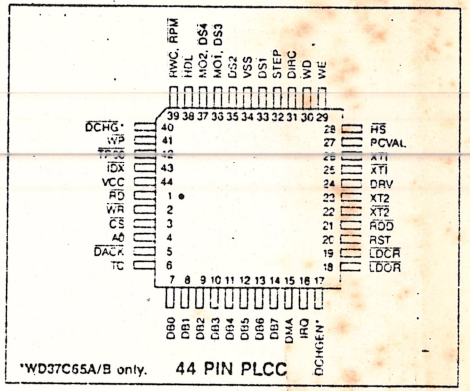
WD37C65/A/B
Floppy Disk Subsystem Controller

FEATURES

- IBM* PC AT* compatible format (single and double density)
  - — Floppy control and operations on chip
  - — In PC AT mode, provides required signal qualification to DMA channel
  - — BIOS compatible
  - — Dual speed spindle drive support
- Address mark detection circuitry internal to floppy disk controller
- Multisector and multitrack transfer capability
- Direct floppy disk drive interface with no buffers needed
  - — 48mA sink output drivers
  - — Schmitt Trigger line receivers
- Compatible with PD8080/85, PD8086, and PD780 (Z80™) microprocessors
- On chip clock generation
- Two TTL clock inputs for 40 pin DIP
- Two XTAL oscillator circuits for 44 pin PLCC
- Automatic write precompensation
- Inner track value of 125 or 187NS pin selectable
- Enhanced host interface
  - — Read/Write accesses compatible registers with 8 or 12 MHz 286 microprocessor with 0 wait states
  - — 20 LSTTL output drive capability
  - — Inputs are TTL level Schmitt Trigger (except data bus)
  - — DMA timing corrected
- User programmable track stepping rate and head load/unload time
- Drives up to four floppy or Micro Floppydisk™ drives
- Data transfer in DMA or non-DMA mode
- Parallel seek operations on up to four drives
- Internal power up reset circuitry (WD37C65A/B only).
- High performance, classical 2nd order, type 2, phase locked loop digital data separator <10E-9 industry standard error rate
- 125, 250, 300, 500 kbits/sec data rates
- CMOS low power 125mW
- +5V DC power supply



40 PIN DIP



*WD37C65A/B only. 44 PIN PLCC

DESCRIPTION

The WD37C65/A/B Floppy Disk Subsystem Controller is an LSI device that provides all the needed functionality between the host processor peripheral bus and the cable connector to the floppy disk drive. This "superchip" intergrates: formatter/controller, data separation, write precompensation, data rate selection, clock generation, drive interface drivers and receivers.

WD37C65/A/B is a reference to the fact that there are three revisions of this device: the original WD37C65, the WD37C65A, and the WD37C65B. The WD37C65A and the WD37C65B are pin-for-pin compatible with the WD37C65, except for the 44 pin PLCC package, where advantage was taken of the additional pins. The only difference between the WD37C65A and the WD37C65B is the fact

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Micro Floppydisk is a registered trademark of Sony Corporation.

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that the WD37C65A (and the WD37C65) issues 255 step pulses, while the WD37C65B issues 77 step pulses during a recalibrate command. In the WD37C65A/B, pins 17 and 40, which were not utilized in the WD37C65, became $\overline{DCHGEN}$ (Disk CHanGe ENable) and $\overline{DCHG}$ (Disk CHanGe) respectively. Both are active low. $\overline{DCHGEN}$ is offered as an option for those designs that used the original WD37C65 part where $\overline{DCHG}$ did not exist as a direct input into the chip.

On the disk drive interface, the WD37C65/A/B includes data separation that has been designed to address high performance error rates on floppy disk drives, and contains all the necessary logic to achieve classical 2nd order, type 2, phase locked loop performance. Write precompensation is included, in addition to the usual formatting, encoding/decoding, stepper motor control, and status sensing functions. All inputs are TTL compatible Schmitt Trigger line receivers, and outputs are high current, open drain, with the 48 mA drivers meeting the ANSI specification.

The host interface has been improved for speed operation supporting eight or 12 MHz, 286 microprocessor bus without the use of wait states. The inputs are Schmitt Triggers (except the data bus). Output drive capability is 20 LSTTL loads, allowing direct interconnection to bus structures without the use of buffers or transceivers. For PC and PC AT applications, qualification of interrupt request and DMA request is provided.

Traditionally, data rate selection, drive selection, and stepper motor control have been output ports of the host processor architecture. In the WD37C65/A/B, these functions are latched into registers addressed within the I/O mapping of the system. The WD37C65/A/B has eight internal registers. The eight bit main status register

(Continued on page 5).

PIN DESCRIPTIONS

D/P PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
1/1	$\overline{RD}$	$\overline{READ}$	I	Control signal for transfer of data or status onto the data bus by the WD37C65/A/B.
2/2	$\overline{WR}$	$\overline{WRITE}$	I	Control signal for latching data from the bus into the WD37C65/A/B Buffer Register.
3/3	$\overline{CS}$	$\overline{CHIP\ SELECT}$	I	Selected when 0 (low) allowing $\overline{RD}$ or $\overline{WR}$ operation from the host.
4/4	A0	ADDRESS LINE	I	Address line selecting data (=1) or status (=0) information. (A0 = logic 0 during $\overline{WR}$ is illegal).
5/5	$\overline{DACK}$	$\overline{DMA\ ACKNOWLEDGE}$	I	Used by the DMA controller to transfer data from the WD37C65/A/B onto the bus. Logical equivalent to $\overline{CS}$ and A0=1. In Special or PC AT mode, this signal is qualified by DMAEN from the Operations Register.
6/6	TC	TERMINAL COUNT	I	This signal indicates to WD37C65/A/B that data transfer is complete. If DMA operational mode is selected for command execution, TC will be qualified by $\overline{DACK}$, but not in the programmed I/O execution. In PC AT or Special mode, qualification by $\overline{DACK}$ requires the Operations Register signal DMAEN to be logically true. Note also that in PC AT mode, TC will be qualified by $\overline{DACK}$, whether in DMA or non-DMA host operation. Programmed I/O in PC AT mode will cause an abnormal termination error at the completion of a command.
7-14 7-14	DB0 thru DB7	DATA BUS 0 thru DATA BUS 7	I/O	8-Bit, bi-directional, tri-state, data bus. D0 is the least significant bit (LSB). D7 is the most significant bit (MSB).
15/15	DMA	DIRECT MEMORY ACCESS	O	DMA request for byte transfers of data. In Special or PC AT mode, this pin is tri-stated, enabled by the DMAEN signal from the Operations Register. This pin is driven in the Base mode.
16/16	IRQ	INTERRUPT	O	Interrupt request indicating the completion of command execution or data transfer requests (in non-DMA mode). Normally, ... in base mode. In Special or PC AT mode, this pin is tri-stated, enabled by the DMAEN signal from the Operations Register.

PIN DESCRIPTIONS (cont.)

D/P PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
17	$\overline{DCHGEN}$*	$\overline{DISK\ CHANGE\ ENABLE}$	I	This input must be at Logic = 0 to enable $\overline{DCHG}$ input status at pin 40 to be placed on DB7 during a $\overline{RD}$ = 0 of $\overline{LDCR}$ = 0. Internal pull-up.
17/18	$\overline{LDOR}$	$\overline{LOAD\ OPERATIONS\ REGISTER}$	I	Address decode which enables the loading of the Operations Register. Internally gated with $\overline{WR}$ creates the strobe which latches the data bus into the Operations Register.
18/19	$\overline{LDCR}$	$\overline{LOAD\ CONTROL\ REGISTER}$	I	Address decode which enables loading of the Control Register. Internally gated with $\overline{WR}$ creates the strobe which latches the two LSBs from the data bus into the Control Register.
19/20	RST	RESET	I	Resets controller, placing microsequencer in idle. Resets device outputs. Puts device in Base mode, not PC AT or Special mode.
20/21	$\overline{RDD}$	$\overline{READ\ DISK\ DATA}$	I	This is the raw serial bit stream from the disk drive. Each falling edge of the pulses represents a flux transition of the encoded data.
21/	CLK2	CLOCK2	I	TTL level clock input used for non-standard data rates; is 9.6MHz for 300 kbs, and can only be selected from the Control Register.
/22	$\overline{XT2}$	$\overline{XTAL2}$	O	XTAL oscillator drive output for 44 pin PLCC (See Figure 6). Should be left floating if TTL inputs used at pin 23.
/23	XT2	XTAL2	I	XTAL oscillator input used for non-standard data rates. It may be driven with a TTL level signal.
22/24	DRV	DRIVE TYPE	I	Drive type input indicates to the device that a two-speed spindle motor is used if logic is 0. In that case, the second clock input will never be selected and must be grounded.
23/	CLK1	CLOCK1	I	TTL level clock input is used to generate all internal timings for standard data rates. Frequency must be 16MHz ± 0.1%, and may have 40/60 or 60/40 duty cycle.
/25	$\overline{XT1}$	$\overline{XTAL1}$	O	XTAL oscillator drive output for 44 pin PLCC (See Figure 6). Should be left floating if TTL inputs used at pin 26.
/26	XT1	XTAL1	I	XTAL oscillator input requiring 16MHz crystal. This oscillator is used for all standard data rates, and may be driven with a TTL level signal.
24/27	PCVAL	PRECOMPENSATION VALUE	I	PRECOMPENSATION VALUE select input. This pin determines the amount of write precompensation used on the inner tracks of the diskette. Logic 1 = 125ns. Logic 0 = 187ns.
25/28	$\overline{HS}$	$\overline{HEAD\ SELECT}$	O	High current driver (HCD) output selects the head (side) of the floppy disk that is being read or written. Logic 1 = side 0. Logic 0 = side 1.
26/29	$\overline{WE}$	$\overline{WRITE\ ENABLE}$	O	This HCD output becomes true, active low, just prior to writing on the diskette. This allows current to flow through the write head.
27/30	$\overline{WD}$	$\overline{WRITE\ DATA}$	O	This HCD output is $\overline{WRITE\ DATA}$. Each falling edge of the encoded data pulse stream causes a flux transition on the media.

*Only in the PLCC version of the WD37C65A/B. Not connected in the WD37C65.

PIN DESCRIPTIONS (cont.)

D/P PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
28/31	$\overline{DIRC}$	$\overline{DIRECTION}$	O	This HCD output determines the direction of the head stepper motor. Logic 1 = outward motion. Logic 0 = inward motion.
29/32	$\overline{STEP}$	$\overline{STEP\ PULSE}$	O	This HCD output issues an active low pulse for each track to track movement of the head.
30/33	$\overline{DS1}$	$\overline{DRIVE\ SELECT\ 1}$	O	This HCD output, when active low, is $\overline{DRIVE\ SELECT\ 1}$ in PC AT mode, enables the interface in this disk drive. This signal comes from the Operations Register. In Base, or Special mode, this output is #1 of the four decoded Unit Selects, as specified in the device command syntax.
31/34	VSS	GROUND		Ground.
32/35	$\overline{DS2}$	$\overline{DRIVE\ SELECT\ 2}$	O	This HCD output, when active low, is $\overline{DRIVE\ SELECT\ 2}$ in PC AT mode, enables the interface in this disk drive. This signal comes from the Operations Register. In Base or the Special mode, this output is #2 of the four decoded Unit Selects as specified in the device command syntax.
33/36	$\overline{MO1}$, $\overline{DS3}$	$\overline{MOTOR\ ON\ 1}$, $\overline{DRIVE\ SELECT\ 3}$	O	This HCD output, when active low, is MOTOR ON enable for disk drive #1, in PC AT mode. This signal comes from the Operations Register. In the Base or Special mode, this output is #3 of the four decoded Unit Selects as specified in the device command syntax.
34/37	$\overline{MO2}$, $\overline{DS4}$	$\overline{MOTOR\ ON\ 2}$, $\overline{DRIVE\ SELECT\ 4}$	O	This HCD output, when active low, is MOTOR ON enable for disk drive #2, in PC AT mode. This signal comes from the Operations Register. In the Base or Special mode. this output is #4 of the four decoded Unit Selects as specified in the device command syntax.
35/38	$\overline{HDL}$	$\overline{HEAD\ LOADED}$	O	This HCD output, when active low, causes the head to be loaded against the media in the selected drive.
36/39	$\overline{RWC}$, $\overline{RPM}$	$\overline{REDUCED\ WRITE\ CURRENT}$, $\overline{REVOLUTIONS\ PER\ MINUTE}$	O	This HCD output, when active low, causes a $\overline{REDUCED\ WRITE\ CURRENT}$ when bit density is increased toward the inner tracks, becoming active when tracks > 28 are accessed. This condition is valid for Base or Special mode, and is indicative of when write precompensation is necessary. In the PC AT mode, this signal will be active when CR0=1.
40	$\overline{DCHG}$	$\overline{DISK\ CHANGE}$	I	This ST input senses status from the drive, indicating active low that drive door is open or that the diskette has possibly changed since last drive selection.
37/41	$\overline{WP}$	$\overline{WRITE\ PROTECTED}$	I	This Schmitt Trigger (ST) input senses status from the disk drive, indicating active low when a diskette is $\overline{WRITE\ PROTECTED}$.
38/42	$\overline{TR00}$	$\overline{TRACK\ 00}$	I	This ST input senses status from disk drive, indicating active low when the head is positioned over the outermost track, $\overline{TRACK\ 00}$.
39/43	$\overline{IDX}$	$\overline{INDEX}$	I	This ST input senses status from the disk drive, indicating active low when the head is positioned over the beginning of a track marked by an index hole.
40/44	VCC	+5VDC		Input power supply.

Only in the PLCC version of the WD37C65A/B. Not connected in the WD37C65.

contains status information of the WD37C65/A/B and may be accessed any time. Another four status registers under system control also give various status and error information. The Control Register provides support logic that latches the two LSBs used to select the desired data rate that controls internal clock generation. The Operations Register replaces the standard latched port used in floppy subsystems. These registers are incorporated into the WD37C65/A/B.

All Clock Generation: SCLK – Sampling Clock, WCLK – Write Clock, and MCLK – Master Clock, are included in the WD37C65/A/B. XTAL oscillator circuits provide the necessary signals for internal timing when using the 44 pin PLCC. If the 40 pin DIP is used, the TTL level clock inputs must be provided. There are two oscillator inputs to the WD37C65/A/B; one at 16 MHz that handles all standard data rates (500, 250, and 125 kb/Sec). The other oscillator is at 9.6 MHz to support th rate used in PC AT designs.

Some AT compatibles use two-speed c speed disk drive is used, the DRV grounded along with the CLK2 inpu

ARCHITECTURE

The WD37C65/A/B Floppy Disk Subsy an LSI device that provides all the ne between the host processor peripheral connector to the floppy disk drive. integrates: formatter/controller, data precompensation, data rate selection, drive interface drivers and receivers.

Figure 1 illustrates a block diagram of Floppy Disk Subsystem Controller.

Figure 2 illustrates a typical WD37C6

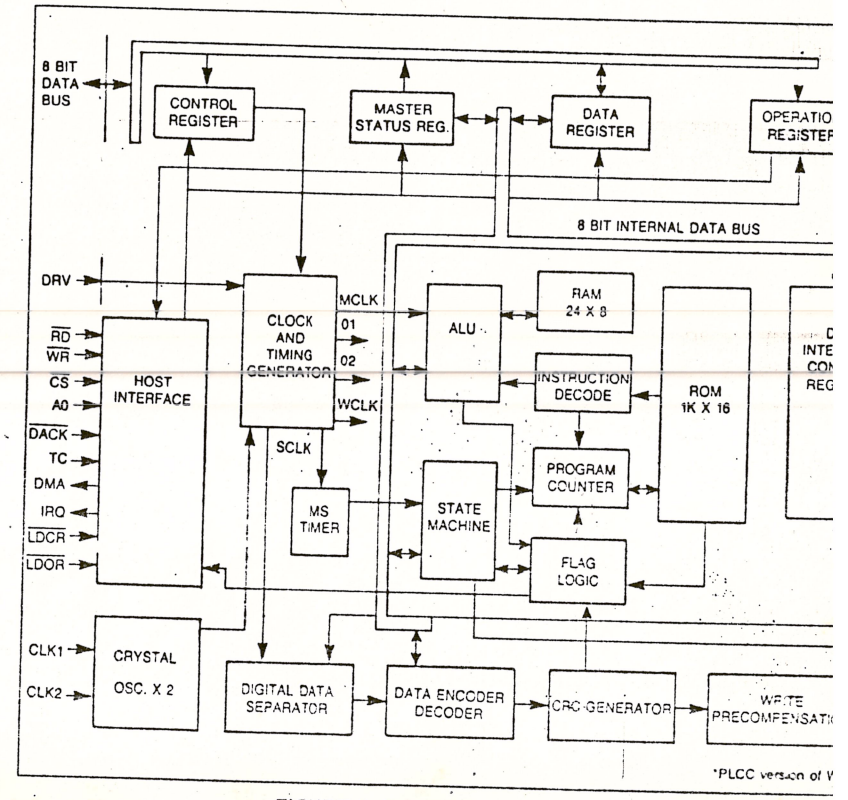

FIGURE 1. WD37C65/A/B BLOCK DIAGRAM

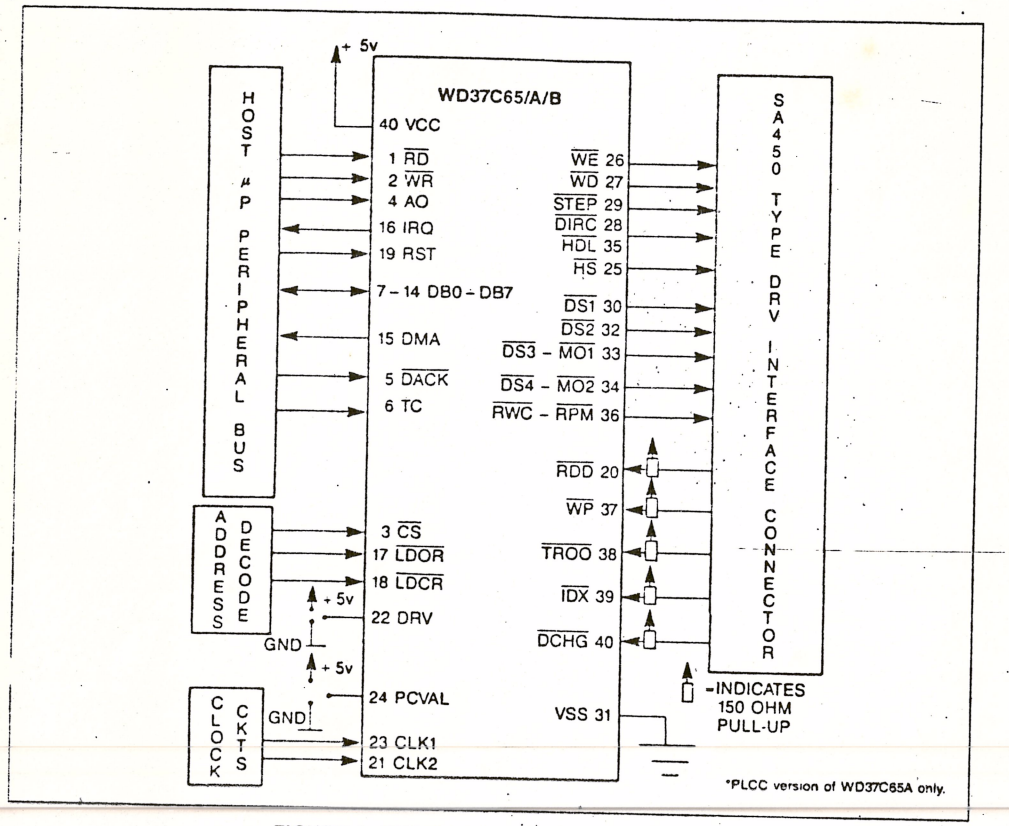

FIGURE 2. TYPICAL WD37C65/A/B SYSTEM

HOST INTERFACE

The host interface is the Host Microprocessor Peripheral Bus. This bus is composed of eight control signals and eight data signals. In the Special or PC AT modes, IRQ and DMA request are tri-stated and qualified by DMA enable, internally provided by the Operations Register. The data bus, DMA, and IRQ outputs are designed to handle 20 LSTTL loading. Inputs, except the data bus, are Schmitt Trigger receivers and can be hooked up to a bus or backplane without any additional buffering.

During the Command or Result phases, the Main Status Register must be read by the processor before each byte of information is written into or read from the Data Register. After each byte of data is read from or written into the Data Register, the CPU should wait for 12μs before reading the Main Status Register. Bits D6 and D7 in the Main Status Register must be in a 0 and 1 state, respectively, before each byte of the command word may be written into the WD37C65/A/B. Many of the commands require multiple bytes. As a result, the Main Status Register must be read prior to each byte transfer to the WD37C65/A/B. During the Result phase, Bits D6 and D7 in the Main Status Register must both be 1's (D6 = 1 and D7 = 1) before reading each byte from the Data Register. Note that this reading of the Main Status Register before each byte transfer to the WD37C65/A/B is required only in the Command and Result phases, and not during the Execution phase. Note also that DB6 and DB7 in the MSR can be polled instead of waiting 12μs. When they have the right bit settings, the WD37C65/A/B is ready for commands. This might save some time.

During the Execution phase, the Main Status Register need not be read. If the WD37C65/A/B is in the non-DMA Mode, then the receipt of each data byte (WD37C65/A/B is reading data from the FDD) is indicated by an interrupt signal on pin 16 (IRQ = 1). The generation of a Read signal ($\overline{RD}$ = 0) will clear the interrupt as well as output the data onto the data bus. If the processor cannot handle interrupts fast enough (every 13μs for the MFM mode and 27μs for the FM mode), then it may poll the Main Status Register and bit D7 (RQM) functions as the Interrupt signal. If a Write Command is in process then the $\overline{WR}$ signal performs the reset to the Interrupt signal.

All timings mentioned above double for mini floppy data rates.

Note that in the non-DMA mode it is necessary to examine the Main Status Register to determine the cause of the interrupt since it could be a data interrupt or a command termination interrupt, either normal or abnormal. If the WD37C65/A/B is in the DMA mode, no Interrupt signals are generated during the Execution phase. The WD37C65/A/B generates DMA's (DMA Requests) when each byte of data is available. The DMA Controller responds to this request with both $\overline{DACK}$ = 0 (DMA Acknowledge) and an $\overline{RD}$ = 0 (Read signal). When the DMA Acknowledge signal goes low ($\overline{DACK}$ = 0), then the DMA Request is cleared (DMA = 0). If a Write Command has been issued, then a $\overline{WR}$ signal will appear instead of $\overline{RD}$. After the Execution phase has been completed (Terminal Count has occurred) or the EOT sector read/written, then an Interrupt will occur (IRQ = 1). This signifies the beginning of the Result phase. When the first byte of data is read during the Result phase, the Interrupt is automatically cleared (IRQ = 0).

It should be noted that in PC AT usage, non-DMA Host transfers are not the normal procedure. If the user chooses to do so, the WD37C65/A/B will successfully complete commands, but will always give abnormal termination error status since TC is qualified by an inactive $\overline{DACK}$.

The $\overline{RD}$ or $\overline{WR}$ signals should be asserted while $\overline{DACK}$ is true. The $\overline{CS}$ signal is used in conjunction with $\overline{RD}$ and $\overline{WR}$ as a gating function during programmed I/O operations. $\overline{CS}$ has no effect during DMA operations. If the non-DMA mode is chosen, the $\overline{DACK}$ signal should be pulled up to Vcc. It is important to note that during the Result phase all bytes shown in the Command Table must be read. The Read Data Command for example, has several bytes of data in the Result phase. All seven bytes must be read in order to successfully complete the Read Data command. The WD37C65/A/B will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the Result phase. The WD37C65/A/B contains five Status Registers. The Main Status Register mentioned may be read by the processor at any time. The other four Status Registers (ST0, ST1, ST2, and ST3) are available only during the Result phase and may be read only after completing a command. The particular command that has been executed determines how many of the Status Registers will be read.

The bytes of data which are sent to the WD37C65/A/B to form the Command phase, and are read out of the WD37C65/A/B in the Result phase, must occur in the order shown in the Command Table. The command code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the Command or Result phases is allowed. After the last byte of data in the Command phase is sent to the WD37C65/A/B, the Execution phase automatically starts. In a similar fashion, when the last byte of data is read out in the Result phase, the command is automatically ended and the WD37C65/A/B is ready for a new command.

CONTROL REGISTER

The Control Register provides support logic that latches the two LSBs of the data bus upon receiving $\overline{LDCR}$ and $\overline{WR}$. $\overline{CS}$ should not be active when this happens. These bits are used to select the desired data rate, which in turn controls the internal clock generation. Clock switchover is internally "deglitched," allowing continuous operation after changing data rates. If the Control Register is not used, the data rate is governed by the supplied clock or crystal. The frequency must be 64X the desired MFM data rate, up to a maximum frequency of 16 MHz. This implies a maximum data rate of 250 kb/s, unless the Control Register is used. Switching this clock must be "glitchless" or the device will need to be reset. Table 1 presents the Control Register.

TABLE 1. CONTROL REGISTER

CR1	CR0	DRV	DATA RATE	COMMENTS	RPM (IN PC/AT mode)
0	0	X	500 K	MFM	1
0	0	X	250 K	FM	1
0	1	0	250 K	MFM	0
0	1	1	300 K	MFM	0
1	0	X	250 K	MFM, RST Default	1
1	0	X	125 K	FM, RST Default	1
1	1	X	125 K	FM	0

MASTER STATUS REGISTER

The Master Status Register is an eight-bit register that contains the status information of the FDC, and may be accessed at any time. Only the Master Status Register may be read and used to facilitate the transfer of data between the processor and WD37C65/A/B. The DIO and RQM bits in the Master Status Register indicate when data is ready and in which direction data will be transferred on the data bus. The maximum time between the last $\overline{RD}$ or $\overline{WR}$ during a Command or Result phase and DIO and RQM getting set is 12μs if 500 kb/s MFM data rate is selected. (If 250 kb/s MFM is selected, the delay is 24μs.) For this reason, everytime the Master Status Register is read, the CPU should wait 12μs. The maximum time from the trailing edge of the last $\overline{RD}$ in the result phase to when DB4 (FDC busy) goes low is 12μs.

The bits in the Master Status Register are listed in Table 2.

TABLE 2. MASTER STATUS REGISTER BITS

BIT NO.	NAME	SYMBOL	DESCRIPTION
DB0	FDD 0 BUSY	D0B	FDD number is 0 in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE commands.
DB1	FDD 1 BUSY	D1B	FDD number 1 is in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE commands.
DB2	FDD 2 BUSY	D2B	FDD number 2 is in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE commands.
DB3	FDD 3 BUSY	D3B	FDD number 3 is in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE commands.
DB4	FDC BUSY	CB	A READ or WRITE command is in progress. FDC will not accept any other command.
DB5	EXECUTION MODE	EXM	This bit is set only during Execution phase in non-DMA mode. When DB5 goes low Execution phase has ended and Results Phase has started. It operates only during non-DMA mode of operation.
DB6	DATA INPUT	DIO	Indicates direction of data transfer between FDC and Data Register. If DIO=1, then transfer is from Data Register to the processor. If DIO=0, then transfer is from the processor to Data Register.
DB7	REQUEST FOR MASTER	RQM	Indicates Data Register is ready to send or receive data to or from the processor. Both bits DIO and RQM should be used to perform the handshaking functions of "ready" and "direction" to the processor.

in Status Register 0 are listed in Table 3.

ABLE 3. STATUS REGISTER 0 BITS

BIT NO.	NAME	SYMBOL	DESCRIPTION
			D7=0 and D6=0. Normal termination of command was completed and properly executed.
D7	INTERRUPT CODE	IC	D7=0 and D6=1. Abnormal termination of command, (AT). Execution of command was started but was not successfully completed.
D6			D7=1 and D6=0. Invalid command issue, (IC). Command which was issued was never started.
D5	SEEK END	SE	When the FDC completes the SEEK command, this flag is set to 1 (high).
†D4	EQUIPMENT CHECK	EC	If the Track 0 signal fails to occur after 255 step pulses (Recalibrate Command), then this flag is set.
†D3	NOT READY	NR	Since drive Ready is always presumed true, this will always be a logic 0.
D2	HEAD SELECT	HS	This flag is used to indicate the state of the head at interrupt.
D1	UNIT SELECT 1	US1	This flag is used to indicate a Drive Unit Number at interrupt.
D0	UNIT SELECT 0	US0	This flag is used to indicate a Drive Unit Number at interrupt.

The bits in Status Register 1 are listed in Table 4.

TABLE 4. STATUS REGISTER 1 BITS

BIT NO.	NAME	SYMBOL	DESCRIPTION
D7	END OF CYLINDER	EN	When the FDC tries to access a sector beyond the final sector of a cylinder, this flag is set.
D6			Not used. This bit is always 0 (low).
D5	DATA ERROR	DE	When the FDC detects a *CRC error in either the ID field or the data field, this flag is set.
D4	OVERRUN	OR	If the FDC is not serviced by the host system during data transfers within a certain time interval, this flag is set.
D3			Not used. This bit is always 0 (low).
D2	NO DATA	ND	During execution of READ DATA, WRITE DELETED DATA, or SCAN command, if the FDC cannot find the sector specified in the **IDR Register, this flag is set. During execution of the READ ID command, if the FDC cannot read the ID field without an error, then this flag is set.
			During execution of the READ A TRACK command, if the starting sector cannot be found, then this flag is set.
D1	NOT WRITEABLE	NW	During execution of WRITE DATA, WRITE DELETED DATA or FORMAT A TRACK commands, if the FDC detects a $\overline{WP}$ signal from the FDD, then this flag is set.
D0	MISSING ADDRESS MARK	MA	If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set.
			If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. At the same time the MD (Missing Address Mark in data field) of Status Register 2 is set.

The bits in Status Register 2 are listed in Table 5.

TABLE 5. STATUS REGISTER 2 BITS

BIT NO.	NAME	SYMBOL	DESCRIPTION
D7			Not Used. This bit is always 0 (low).
D6	CONTROL MARK	CM	During execution of the READ DATA or SCAN Command, if the FDC encounters a sector which contains a Deleted Data Address Mark, this flag is set.
D5	DATA ERROR	DD	If the FDC detects a CRC error in the data field, then this flag is set.
D4	WRONG CYLINDER	WC	This bit is related to the ND bit, and when the contents of ***C on the medium is different from that stored in the IDR, this flag is set.
D3	SCAN EQUAL	SH	During execution of the SCAN command, if the condition of "equal" is satisfied, this flag is set.
D2	SCAN NOT	SN	During execution of the SCAN command, if the FDC cannot find a sector on the cylinder which meets the condition, then this flag is set.
D1	BAD CYLINDER	BC	This bit is related to the ND bit, and when the contents of C on the medium is different from that stored in the IDR and the contents of C is FF, then this flag is set.
D0	MISSING ADDRESS MARK IN DATA FIELD	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set.

The bits in Status Register 3 are listed in Table 6.

TABLE 6. STATUS REGISTER 3 BITS

BIT NO.	BIT NAME	BIT SYMBOL	DESCRIPTION
†D7	–	–	Not used. Will always be logic 0.
D6	WRITE PROTECTED	$\overline{WP}$	This bit is used to indicate the status of the WRITE PROTECTED signal from the FDD.
†D5	READY	RY	This bit will always be a logic 1. Drive is presumed to be ready.
D4	TRACK 0	T0	This bit is used to indicate the status of the Track 0 signal from the FDD.
†D3	WRITE PROTECTED	$\overline{WP}$	This bit is used to indicate the status of the WRITE PROTECTED signal from the FDD.
D2	HEAD SELECT	HS	This bit is used to indicate the status of the Side Select signal to the FDD.
D1	UNIT SELECT 1	US1	This bit is used to indicate the status of the Unit Select 1 signal to the FDD.
D0	UNIT SELECT 2	US0	This bit is used to indicate the status of the Unit Select 0 signal to the FDD.

* CRC - Cyclic Redundancy Check
** IDR - Internal Data Register
*** C - Cylinder
† - Different from NEC765

DATA REGISTER

The eight-bit Data Register stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the Data Register in order to program or obtain the results after a particular command.

The relationship between the Master Status Register and the Data Register and the signals $\overline{RD}$, $\overline{WR}$, and A0 are shown in Table 7.

TABLE 7. MASTER STATUS AND DATA REGISTERS RELATIONSHIP

A0	$\overline{RD}$	$\overline{WR}$	FUNCTION
0	0	1	Read Main Status Register
0	1	0	Illegal
0	0	0	Illegal
1	0	0	Illegal
1	0	1	Read from Data Register
1	1	0	Write into Data Register

OPERATIONS REGISTER

The Operations Register provides support logic that latches the data bus upon receiving $\overline{LDOR}$ and $\overline{WR}$. $\overline{CS}$ should not be active when this happens. The Operations Register replaces the typical latched port found in floppy subsystems used to control disk drive spindle motors and to select the desired disk drive. Table 8 represents the Operations Register.

TABLE 8. OPERATIONS REGISTER

OR0	DSEL	; Drive Select, if low and MOEN1 = 1, then $\overline{DS1}$ is active. If high and MOEN2 = 1, then $\overline{DS2}$ is active, but only in the PC AT mode.
OR1	(X)	; In WD37C65A/B this must be a logic 0 for $\overline{DS1}$ and $\overline{DS2}$ to become active. No defined function in WD37C65.
OR2	$\overline{SRST}$	; Soft reset, active low.
OR3	DMAEN	; DMA enable, active in Special and PC AT modes. Qualifies DMA and IRQ outputs and $\overline{DACK}$ input.
OR4	MOEN1	; Motor On enable, inverted output $\overline{MO1}$ is active only in PC AT mode.
OR5	MOEN2	; Motor On enable, inverted output $\overline{MO2}$ is active only in PC AT mode.
OR6	(X)	; Has no defined function. A spare.
OR7	(MSEL)	; Mode Select. During a soft reset condition, may be used to select between Special mode (1) and PC AT mode (0).

BASE, SPECIAL, AND PC AT MODES

Base, Special, and PC AT modes allow subtle differences which the user may find desirable. The Control Register may be used in any mode without altering functionality.

Base Mode

After a hardware reset, RST active, the WD37C65/A/B will be held in soft reset, $\overline{SRST}$ active, with the normally driven signals, DMA request and IRQ request outputs tri-stated. Base mode may be initiated at this time by a chip access by the host. Although this may be any read or write, it is strongly recommended that the Base mode user's first chip access be a read of the Master Status Register. Once Base mode is entered, the soft reset is released, and IRQ and DMA are driven. Base mode prohibits the use of the Operations Register, hence there can be no qualifying by DMAEN and no soft resets. The Drive Select outputs, $\overline{DS1}$ to $\overline{DS4}$, offer a 1 of 4 decoding of the Unit Select bits resident in the command structure. Pin $\overline{RWC}$ represents Reduce Write Current and is indicative of when write precompensation is necessary.

Special Mode

Special mode allows use of the Operations Register for the DMAEN signal as a qualifier and to do a software driven device reset, $\overline{SRST}$. To enter Special mode, the Operations Register is loaded with (1 X 0 0 X 0 X X), setting mode Select to a logic 1 disabling MOEN1 and MOEN2 and causing $\overline{SRST}$ to be active. Then a read of the Control Register address, $\overline{LDCR}$ and $\overline{RD}$, will set the device into Special mode. The $\overline{DS1}$ through $\overline{DS4}$ is again offered in this mode, as is $\overline{RWC}$.

PC AT Mode

For PC AT compatibility, users will write to the Operations Register, $\overline{LDOR}$ and $\overline{WR}$; this action, performed after a hardware reset, or in the Base mode, initiates PC AT mode. PC AT mode can also be entered from Special mode by loading the Operations Register with (0 X 0 0 X 0 X X), setting Mode Select to a logic 0, disabling MOEN1 and MOEN2, and causing $\overline{SRST}$ to be active. Then a read of the Control Register address sets the device into PC AT mode. The $\overline{DS}$ outputs are now replaced with the DSEL and MOEN signals buffered from the Operations Register. DMAEN and $\overline{SRST}$ are supported and compatible with the current BIOS. $\overline{RWC}$ pin function is now $\overline{RPM}$ so that users with two-speed drives may reduce spindle speed from a nominal 360 revolutions per minute to 300 revolutions per minute when active low, or used to reduce write current when a slower data rate is selected for a given drive. Figure 3 illustrates the relationship among the three modes.

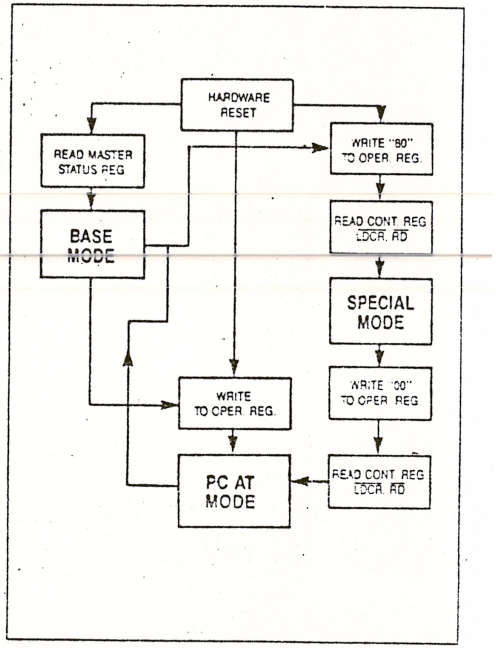

FIGURE 3. FLOW DIAGRAM DEPICTING RELATIONSHIP OF BASE, SPECIAL, AND PC AT MODES.

POLLING ROUTINE

After any reset the WD37C65/A/B, (a hard RST or soft $\overline{SRST}$), will automatically go into a Polling routine. In between commands (and between step pulses in the SEEK Command), the WD37C65/A/B polls all four FDDs looking for a change in the Ready line from any of the drives. Since the drive is always presumed Ready, an interrupt will only be generated following a reset. This occurs because a reset forces Not Ready status, which then promptly becomes Ready. Note that in Special or PC AT modes, if DMAEN is not valid prior to 1ms after reset goes inactive, then IRQ may be already set and pending when finally enabled onto the bus. The polling of the Ready line by the WD37C65/A/B occurs continuously between commands. Each drive is polled every 1.024ms, except during the READ/WRITE commands. For minifloppies, the polling rate is 2.048ms. The drive polling sequence is 1-2-4-3. Please note that in the PC AT mode, the user will not see the polling at the Drive Select signals.

Figure 4 illustrates the Drive Select Polling Timing.

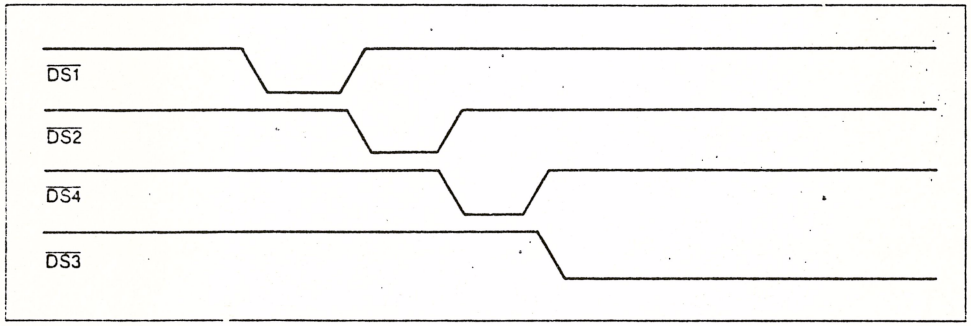

FIGURE 4. DRIVE SELECT POLLING TIMING

DEVICE RESETS

The WD37C65/A/B supports both hardware reset (RST) pin (19) and a software reset ($\overline{SRST}$) through use of the Operations Register. The RST pin will cause a device reset for the active duration. RST causes a default to Base mode, and default selects 250k MFM (or 125k FM, code dependent) as the data rate (16 MHz input clock). $\overline{SRST}$ will reset the microcontroller as did the RST, but will not affect the current data rate selection or the mode. RST, when active, will disable the high current driver outputs to the disk drive. RST and $\overline{SRST}$ will not affect the values set for the internal timers - HUT, HTL, and SRT.

If the XTAL oscillators are used, instead of the TTL driven clock inputs, the hardware RST active time requirement will be extended. The oscillator circuit is designed so that RST will bootstrap the circuit into guaranteed oscillation in a fixed amount of time. The extended reset time allows the growth of the oscillation to produce stable internal clock timing.

DATA SEPARATOR

The Data Separator is a WD92C32 Digital Phase Lock Loop Floppy Disk Data Separator (DPLL). It was designed to address high performance error rates on floppy disk drives, and to provide superior performance in terms of available bit jitter tolerance. It contains the necessary logic to achieve classical 2nd order, type 2, phase locked loop performance. Figure 1 illustrates the WD92C32 used as the Data Separator in the WD37C65/A/B system. Figure 5 illustrates the WD92C32 simplified block diagram. The bit jitter tolerance for the data separator is 60%, which guarantees an error rate of <10E-9.

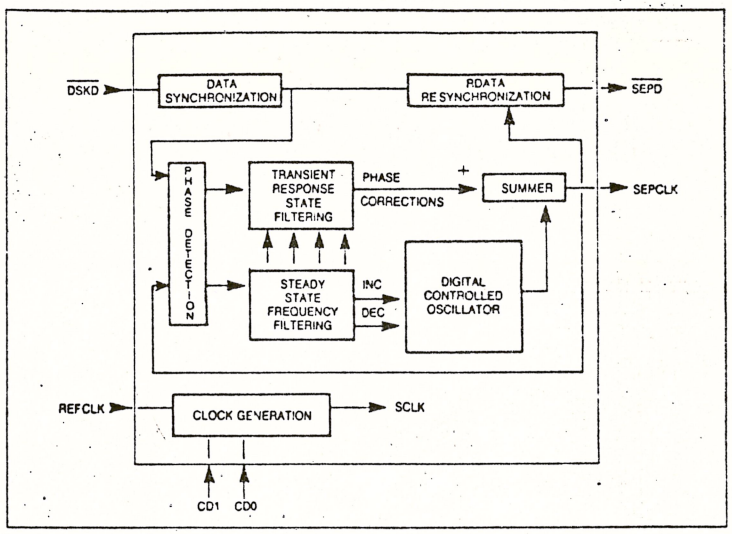

FIGURE 5. WD92C32 SIMPLIFIED BLOCK DIAGRAM

WRITE PRECOMPENSATION

The WD37C65/A/B maintains the standard first level algorithm to determine when write precompensation should be applied. The EARLY and LATE signals are used internally to select the appropriate delay in the write data pulse stream. The encoded WRITE DATA signal is synchronized to the 16 MHz clock if this is the frequency on CLK1 pin (23), and clocked through a shift register. Signals EARLY, NOM, and LATE determine the amount of delay through the shift register before a multiplexer gates the chosen bit to the output. The output data pulse width has a 25% duty cycle, i.e., one fourth of the bit cell period, and equal to one half the WCLK period.

When PCVAL pin (24) = 1, all data will be precompensated by ± 125ns, regardless of track number and data rate. However, this is only for MFM encoding. There is no write precompensation for FM. If PCVAL = 0, and if a track inside number 28 is accessed, then ± 187ns precompensation will be generated. For frequencies other then 16 MHz on the CLK1 pin, the precompensation values will be two and three clock cycles respectively.

When the non-standard data rate using CLK2 is chosen, the MFM precompensation will always be two clock cycles. For 9.6 MHz, this is ± 208ns. In this case, the PCVAL function is disabled.

CLOCK GENERATION

This logical block provides all the clocks needed by the WD37C65/A/B. They are: Sampling Clock (SCLK), Write Clock (WCLK), and the Master Clock (MCLK).

SCLK drives the WD92C32 Data Separator used during data recovery. This clock's frequency is always 32 times the selected data rate.

WCLK is used by the encoder logic to place MFM or FM on the serial WD-stream to the disk. WCLK always has a frequency two times the selected data rate.

MCLK is used by the microsequencer. MCLK and $\overline{MCLK}$ clock all latches in a two-phase scheme. One microinstruction cycle is four MCLK cycles. MCLK has a frequency equal to eight times the selected MFM data rate or 16 times the FM data rate. Table 9 presents the Clock Data Rate. Figure 6 illustrates the XTAL oscillator circuits for the 44 pin PLCC configuration.

TABLE 9. CLOCK DATA RATE

DATA RATE	CODE	SCLK	MCLK	WCLK
500 kb/s	MFM	16.0 MHz	4.0 MHz	1.0 MHz
250 kb/s	FM	8.0 MHz	4.0 MHz	500 KHz
250 kb/s	MFM	8.0 MHz	2.0 MHz	500 KHz
125 kb/s	FM	4.0 MHz	2.0 MHz	250 KHz
300 kb/s	MFM	9.6 MHz	2.4 MHz	600 KHz