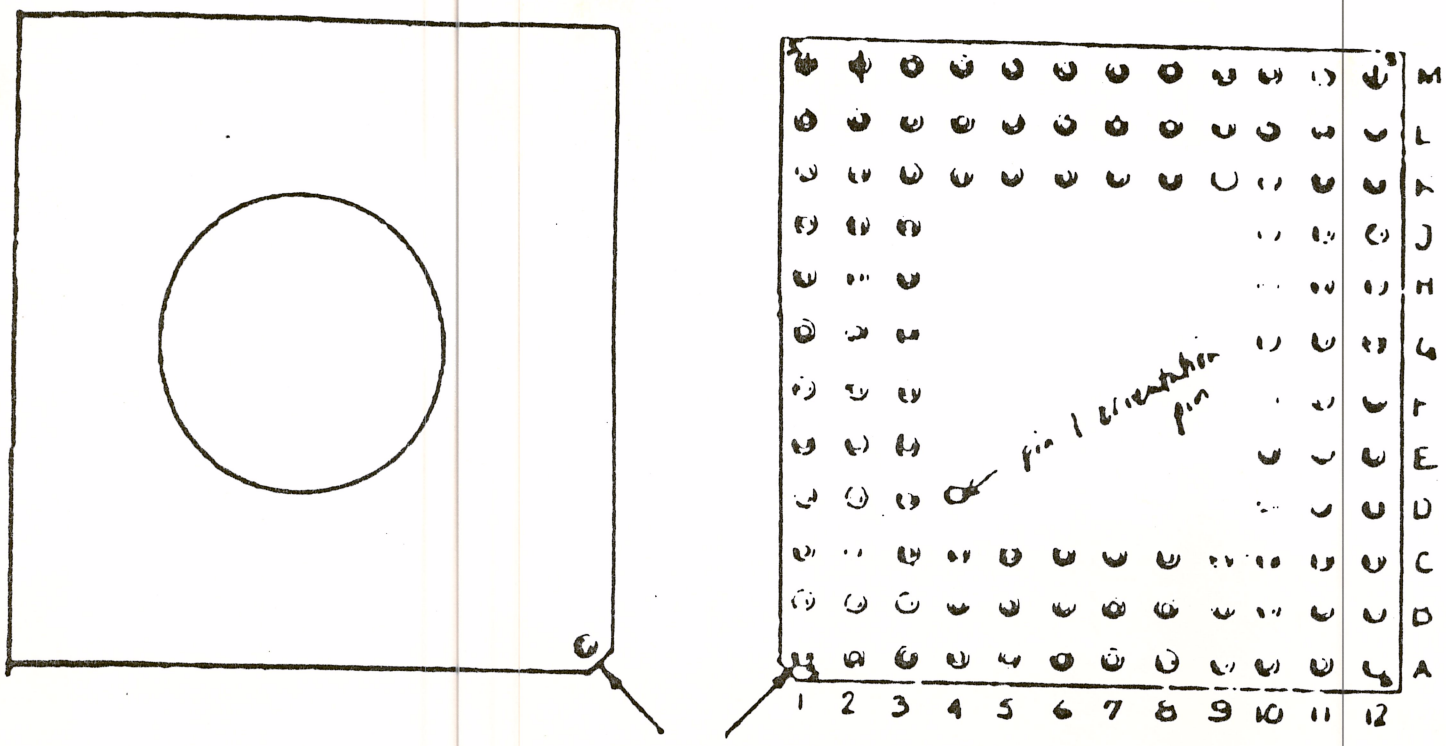
III. Pin Diagram



PIN NUMBER	PIN NUMBER	PIN NUMBER	PIN NUMBER	PIN NUMBER	PIN NUMBER	PIN NUMBER	PIN NUMBER
A1	VSS	C4	INIT	G1	AD5	K10	VDD
A2	STRB	C5	CSA	G2	AD7	K11	S2B
A3	SLCTO	C6	X240	G3	AD6	K12	ALE
A4	CSB	C7	RST	G10	MEMR	L1	SLCTI
A5	EINTA	C8	DNPI	G11	TESTE	L2	ERROR
A6	X24I	C9	X140	G12	BEEP	L3	RAS0
A7	VDD	C10	VDD	H1	AD4	L4	RAS2
A8	CLK4	C11	CLK88	H2	AD3	L5	CSPRP
A9	CLK14	C12	DMAAEN	H3	AD2	L6	IR2
A10	SEMRDI	D1	A16	H10	DEN	L7	IR4
A11	X14I	D2	A18	H11	IOR	L8	DIP1
A12	VSS	D3	ENDVI	H12	MEMW	L9	DIP5
B1	IOCHCK	D10	RDYDMA	J1	AD1	L10	DIP8
B2	WPA	D11	AEN	J2	AD0	L11	KBCK
B3	AUTFD	D12	HOLDA	J3	PE	L12	S0B
B4	DMACS	E1	A14	J10	S1B	M1	VSS
B5	EINTB	E2	A15	J11	DTR	M2	EVENIO
B6	VSS	E3	A17	J12	IOW	M3	RAS1
B7	PWRGD	E10	HRQ	K1	ACK	M4	CAS
B8	CKDMA	E11	RQGT	K2	BUSY	M5	CSPRB
B9	SELFRQ	E12	DACK3	K3	VDD	M6	IR3
B10	IOCRY	F1	A8	K4	MRAS	M7	IR6

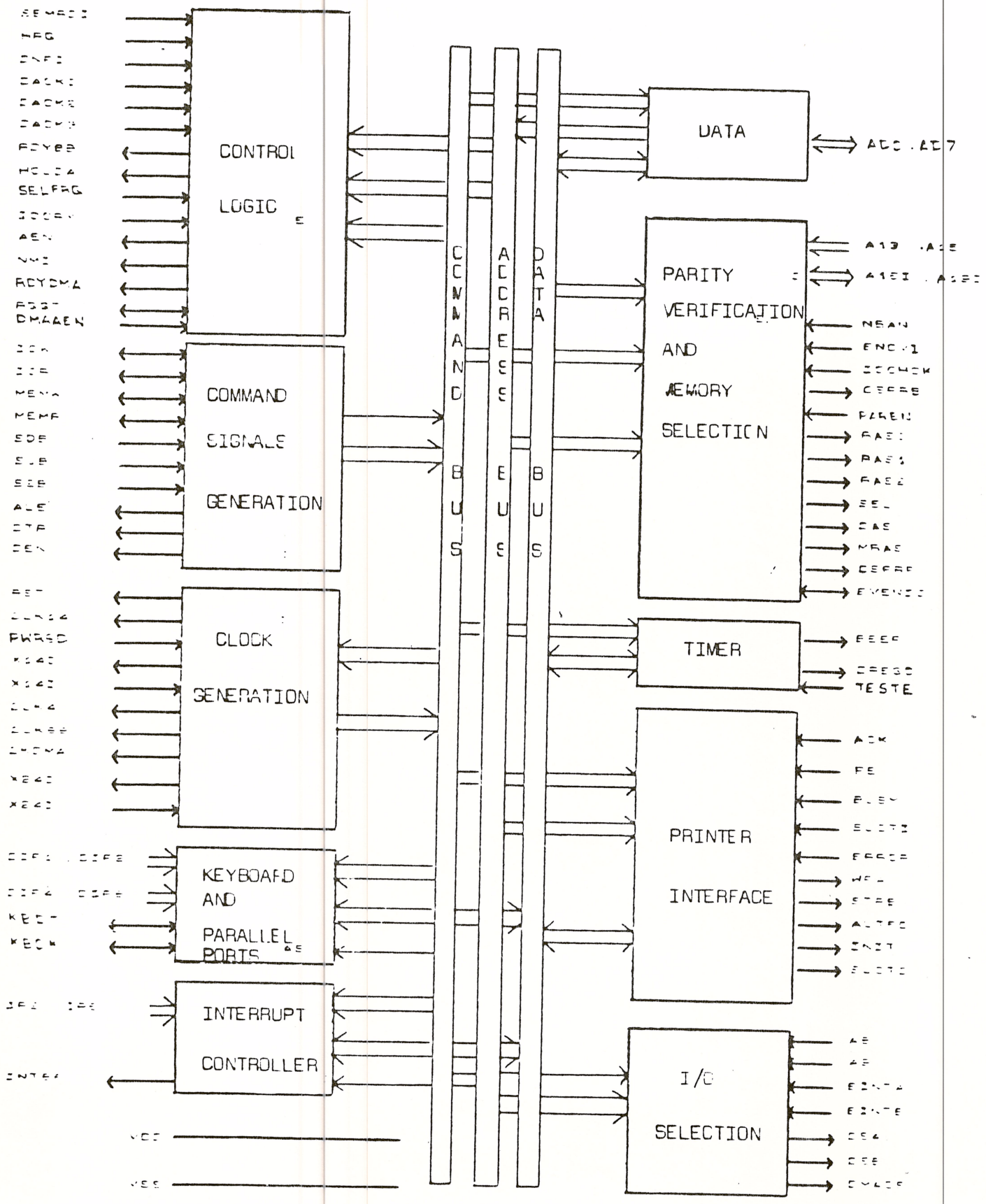
IV. Pin Description

Name	Type	Description
AD0 to AD7	I/O	CPU data and address bus.
A8 to A9 A13 to A15	I	Lines 8, 9, 13, 14 and 15 of the system address bus.
A16 to A19	I/O	Lines 16 to 19 of the CPU address bus.
S0B, S1B, S2B	I	CPU status bits.
ALE	O	Address Latch Enable.
DTR	O	Direction of the CPU data bus driver.
DEN	O	Enable of the CPU data bus driver.
IOR	I/O	I/O read to System and from DMA .
IOW	I/O	I/O write to System and from DMA.
MEMR	I/O	Memory read to System and from DMA.
MEMW	I/O	Memory Write to System and from DMA.
BEEP	O	Tone signal.
DIP1,DIP2, DIP4 to DIP8	I	DIP SWITCHES outputs which indicate the micro-computer configuration.
KBCLK	I/O	Keyboard clock.
KBDT	I/O	Keyboard data.
PWRGD	I	Power Good. Used to generate the system reset.
RST	O	System Reset.
X141 X140	I O	Pins for the connection of the 14.31818 MHz crystal oscillator.

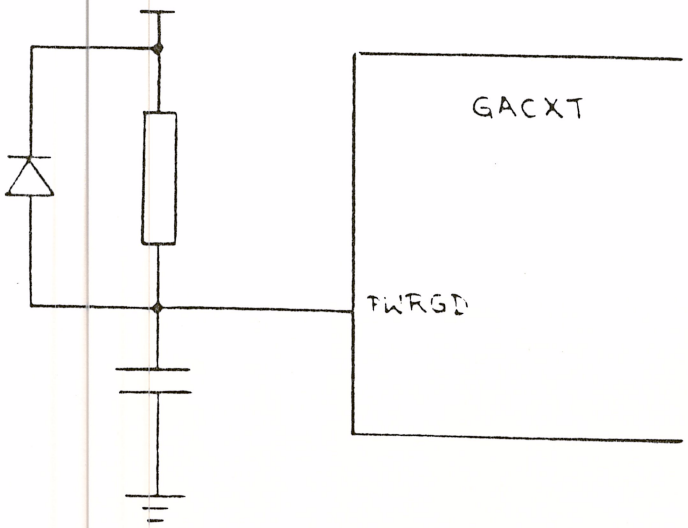
Name	Type	Description
X24I X24O	I O	Pins for the connection of the 20/30 MHz crystal oscillator.
CLK4	O	4.77MHz clock signal, 33% duty cycle.
CLK14	O	14.31818 MHz clock signal.
CLK88	O	CPU clock signal, 33% duty cycle.
CKDMA	O	4.77 MHz, DMA clock signal, 50% duty cycle.
RDY88	O	CPU Ready signal.
IR2I to IR6I	E	Interrupt Request 2 to 6.
INT88	O	Interrupt request signal to CPU.
NMI	O	CPU nonmaskable interrupt.
IOCRY	I	I/O channel ready signal which permits to extend the CPU or DMA access cycles.
IOCHCK	I	Indicates the occurrence of an I/O channel error.
DREQ0	O	DMA Request 0.
DACK0, DACK2, DACK3	I	DMA Acknowledge 0, 2 and 3.
RDYDMA	O	DMA ready signal.
AEN	O	Indicates active DMA.
DMAAEN	O	When DMA is active, this signal activates the drivers of the addresses provided by the DMA.
DNPI	I	Interruption generated by the numerical processor.
SEMRDI	I	Indicates that no CPU wait state is to be generated at pressent access memory instruction for 8/10MHz operation.
EVENIO	I/O	Parity bit from/to memory.
ENDVI	I	Indicates that the maximum addressing capability of the DRAMs is 640 or 704 Kbytes.
NBAN	I	Indicates whether 2 or 3 banks, of 256 Kbytes each are present.

Name	Type	Description
CSPRB	O	Chip Select of the BIOS EPROM.
CSPRP	O	Chip Select of the protection EPROM.
PAREN	I	Disables the parity verification.
RAS0	O	Row Address Strobe of bank 0.
RAS1	O	Row Address Strobe of bank 1.
RAS2	O	Row Address Strobe of bank 2.
SEL	O	Controls the address mux of the DRAMs.
SAS S	O	Column Address Strobe.
MRAS	O	Indicates the selection of the RAM memory controlled by GACXT.
SELFRQ	I	Indicates whether, after reset, the CPU initiates operation at 4.77MHz or 8/10MHz.
HRQ	I	DMA hold request.
HOLDA	O	DMA Hold Acknowledge.
DMACS	O	DMA Chip Select.
RQGT	I/O	Request/Grant 0 to/from CPU.
CSINTA, CSINTB	O	Chip Select of the serial interfaces A and B.
EINTA, EINTB	I	Enables the selection of the serial interfaces A and B.
ACK,PE, BUSY,SLCTI, ERROR	I	Control signals of the parallel interface.
STRB,AUTFD INIT,SLCTO	O	Status signals of the parallel interface.
WPA	O	Controls writing to the data bus of the serial interface.
TESTE	I	When low, GACXT enters test mode. During normal operation, this pin must be tied high.
VDD		+ 5 Volts power supply.
VSS		Ground.

VII. Block Diagram

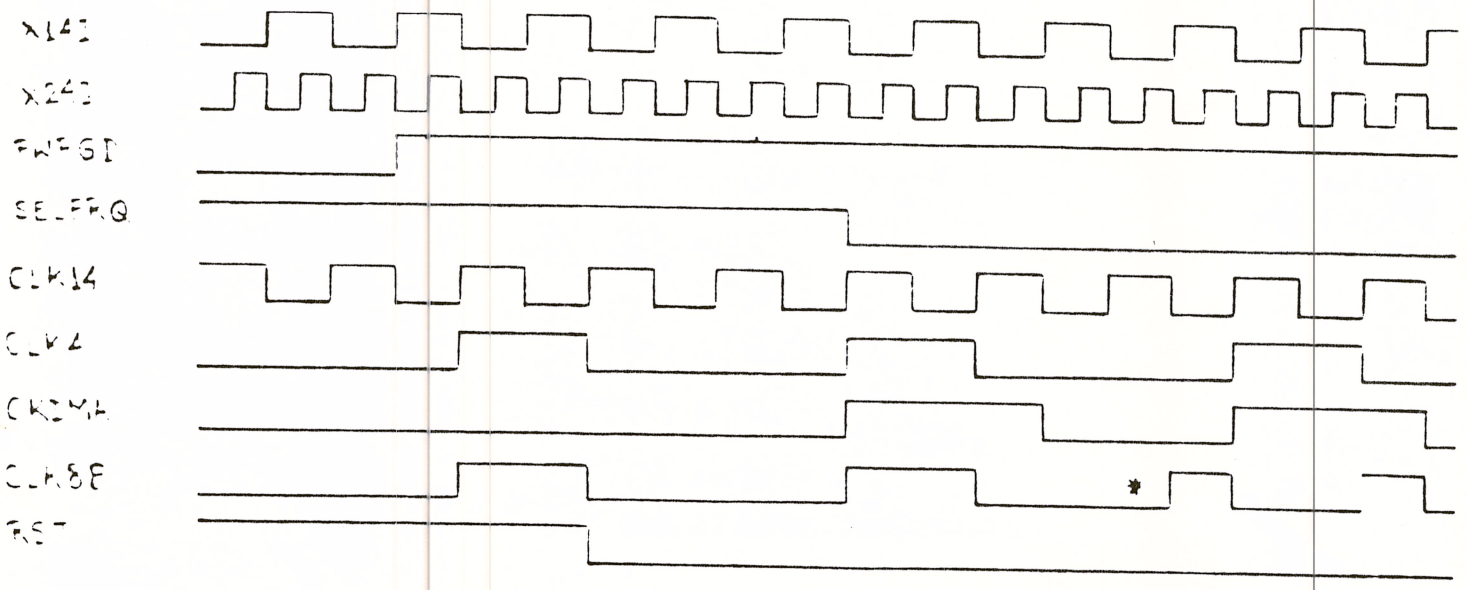


This block generates, as well, the system reset from the PWRGD pin and the 4,77MHz clock signal. The PWRGD pin has a schmitt trigger at its input which permits to couple an RC circuit in order to reset automatically the system when the power supply is activated, as shown by the figure below:



The voltages VT+ and VT- are presented in the section VI (DC Characteristics).

The following figure shows the operation of the preceeding signals:



* CLOCK CHANGE AFTER AT OUT 03C 02H