

# A.C. CHARACTERISTICS—PERIPHERAL (SLAVE) MODE

( $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$ ,  $GND = 0\text{V}$ )

| Symbol | Parameter                                                | 8237A |      | 8237A-4 |      | 8237A-5 |      | Unit |
|--------|----------------------------------------------------------|-------|------|---------|------|---------|------|------|
|        |                                                          | Min.  | Max. | Min.    | Max. | Min.    | Max. |      |
| TAR    | ADR Valid or $\overline{CS}$ LOW to $\overline{RD}$ LOW  | 50    |      | 50      |      | 50      |      | ns   |
| TAW    | ADR Valid to $\overline{WR}$ HIGH Setup Time             | 200   |      | 150     |      | 130     |      | ns   |
| TCW    | $\overline{CS}$ LOW to $\overline{WR}$ HIGH Setup Time   | 200   |      | 150     |      | 130     |      | ns   |
| TDW    | Data Valid to $\overline{WR}$ HIGH Setup Time            | 200   |      | 150     |      | 130     |      | ns   |
| TRA    | ADR or $\overline{CS}$ Hold from $\overline{RD}$ HIGH    | 0     |      | 0       |      | 0       |      | ns   |
| TRDE   | Data Access from $\overline{RD}$ LOW (Note 3)            |       | 200  |         | 200  |         | 140  | ns   |
| TRDF   | $\overline{DB}$ Float Delay from $\overline{RD}$ HIGH    | 20    | 100  | 20      | 100  | 0       | 70   | ns   |
| TRSTD  | Power Supply HIGH to $\overline{RESET}$ LOW Setup Time   | 500   |      | 500     |      | 500     |      | ns   |
| TRSTS  | $\overline{RESET}$ to First $\overline{IOWR}$            | 2TCY  |      | 2TCY    |      | 2TCY    |      | ns   |
| TRSTW  | $\overline{RESET}$ Pulse Width                           | 300   |      | 300     |      | 300     |      | ns   |
| TRW    | $\overline{RD}$ Width                                    | 300   |      | 250     |      | 200     |      | ns   |
| TWA    | ADR from $\overline{WR}$ HIGH Hold Time                  | 20    |      | 20      |      | 20      |      | ns   |
| TWC    | $\overline{CS}$ HIGH from $\overline{WR}$ HIGH Hold Time | 20    |      | 20      |      | 20      |      | ns   |
| TWD    | Data from $\overline{WR}$ HIGH Hold Time                 | 30    |      | 30      |      | 30      |      | ns   |
| TWWS   | Write Width                                              | 200   |      | 200     |      | 160     |      | ns   |

## WAVEFORMS

### SLAVE MODE WRITE TIMING

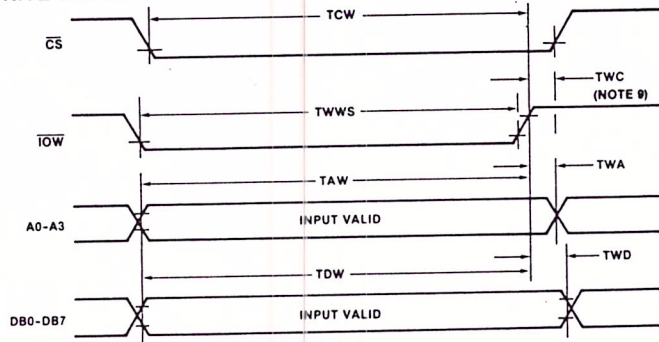


Figure 9. Slave Mode Write

### SLAVE MODE READ TIMING

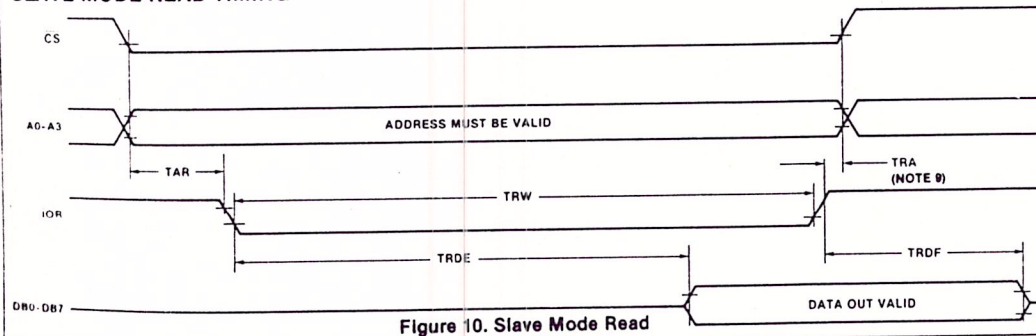


Figure 10. Slave Mode Read



### WAVEFORMS (Continued)

## DMA TRANSFER TIMING

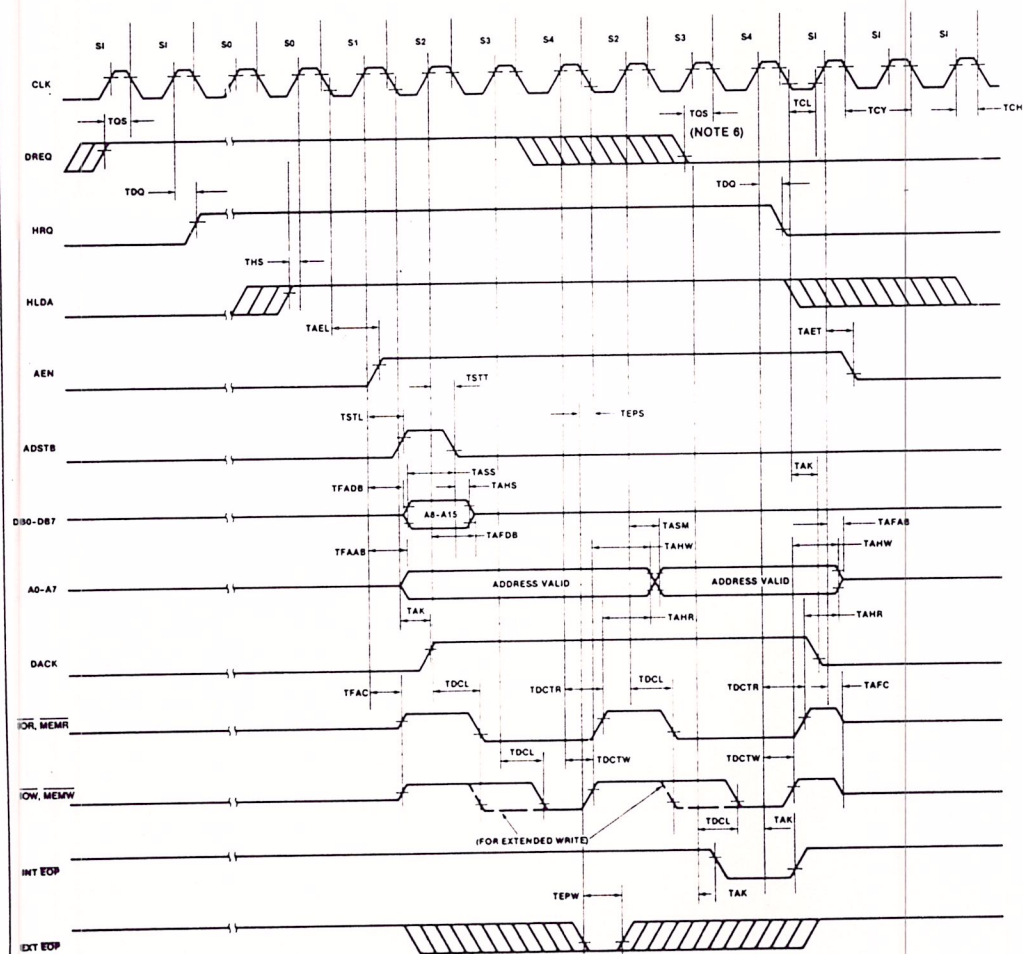


Figure 11. DMA Transfer



WAVEFORMS (Continued)

MEMORY-TO-MEMORY TRANSFER TIMING

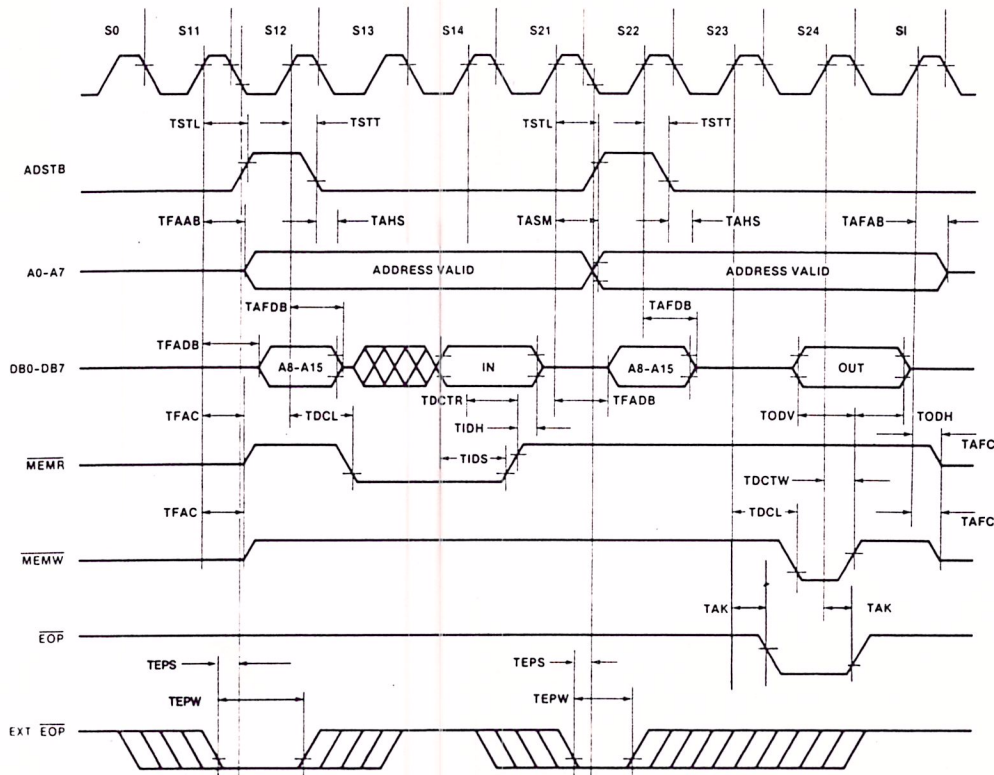


Figure 12. Memory-to-Memory Transfer

READY TIMING

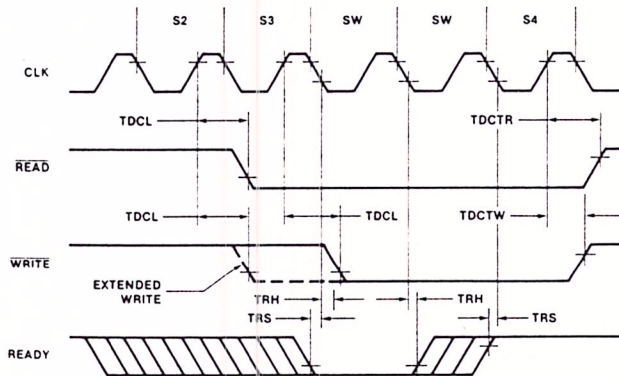


Figure 13. Ready



WAVEFORMS (Continued)

COMPRESSED TRANSFER TIMING

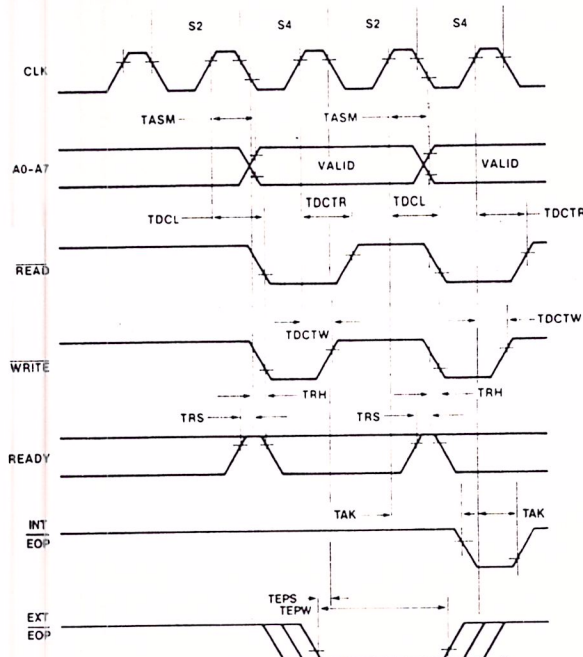


Figure 14. Compressed Transfer

RESET TIMING

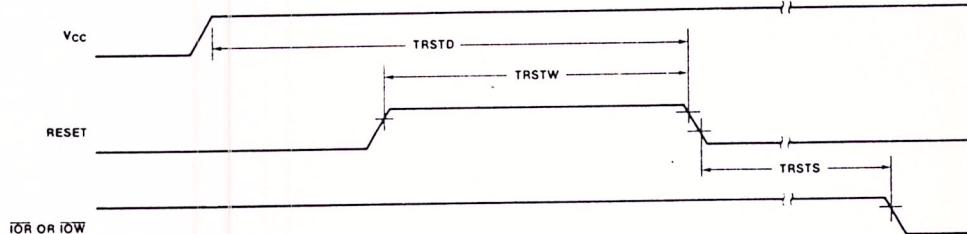


Figure 15. Reset

- MCS-85® C
- 4-Channel I
- Priority DM
- Channel Int
- Terminal Co
- Outputs

The Intel® 8257 is transfer of data a peripheral request from memory. Acc that resolves the count for each ch cycles is complet savings in compo high speed betwe

