Itautec

Lourenço

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type pal1.pgm
PAL16L8


AEN DEN DTR MRES A0 IOW BHE AD0I IORD GND
NC NC D DIRJ GJ GK DIRK GB OCA VCC

/OCA=/AEN*DEN*DTR
/GB=/A0*/DEN*DTR
/GJ=/A0*/MRES+/A0*/AEN+MRES*/DTR*/AEN+MRES*/IOW*/AEN+/IORD*/A0*AEN
/DIRJ=MRES*DEN+/MRES*/AEN+MRES*/A0*DTR+/MRES*IORD*AEN
/GK=A0*/AEN*MRES+AEN*/MRES*A0+/IORD*A0*AEN
/DIRK=DTR*/AEN+/MRES*IORD*AEN
/D=AEN+AD0I+BHE
DESCRIPTION
A)type paltype pal2.pgm
PAL16L8


A0 A1 A2 A3 A4 A5 A6 A7 A8 GND
A9 CSIO AEN IOW LDOR LDCR CSRTC IOR CS37C65 VCC

/LDOR=A9*A8*A7*A6*A5*A4*/A3*/A2*A1*/A0*/AEN
/CS37C65=A9*A8*A7*A6*A5*A4*/A3*A2*/A1*/AEN
/LDCR=A9*A8*A7*A6*A5*A4*/A3*A2*A1*A0*/AEN
/CSRTC=/AEN*A9*/A8*A7*A6*/A5*/IOR+/AEN*A9*/A8*A7*A6*/A5*/IOW
/CSIO=/CSRTC+A9*A7*A6*A5*A4*A3*/AEN+/A9*/A8*/A7*/A6*/A5*/A4*/AEN
DESCRIPTION
A)type pal2m30.pgm
PAL16L8


A0 A1 A2 A3 A4 A5 A6 A7 A8 GND
A9 CSIO AEN IOW LDOR LDCR CSRTC IOR CS37C65 VCC

/LDOR=A9*A8*A7*A6*A5*A4*/A3*/A2*A1*/A0*/AEN
/CS37C65=A9*A8*A7*A6*A5*A4*/A3*A2*/A1*/AEN
/LDCR=A9*A8*A7*A6*A5*A4*/A3*A2*A1*A0*/AEN
/CSRTC=/AEN*/A9*/A8*A7*/A6*A5*A4*/IOR+/AEN*/A9*/A8*A7*/A6*A5*A4*/IOW+/AEN*/A9*/
/CSIO=/CSRTC+A9*A7*A6*A5*A4*A3*/AEN+/A9*/A8*/A7*/A6*/A5*/A4*/AEN
DESCRIPTION
A)type pal3.pgm
PAL14L4


A MEMRD A15 A13 CSPRBO MRAS IORD Q1 SLL GND
MEMWR MEMRES IOWR MRES CSBASIC CSBIOS C CSPROT A14 VCC

/C=/Q1*SLL*IORD*IOWR*/MEMRES+/Q1*SLL*IORD*IOWR*MEMRD*MEMWR
/CSBIOS=/CSPROT+/CSPRBO+A*/A15*/A14*A13*/MEMRD
/CSBASIC=A*/A15*A14*A13+A*A15*/A13+A*A15*/A14
/MRES=/CSPROT+/CSPRBO+A*/A15*/A14*A13*/MEMRD+/MRAS
DESCRIPTION
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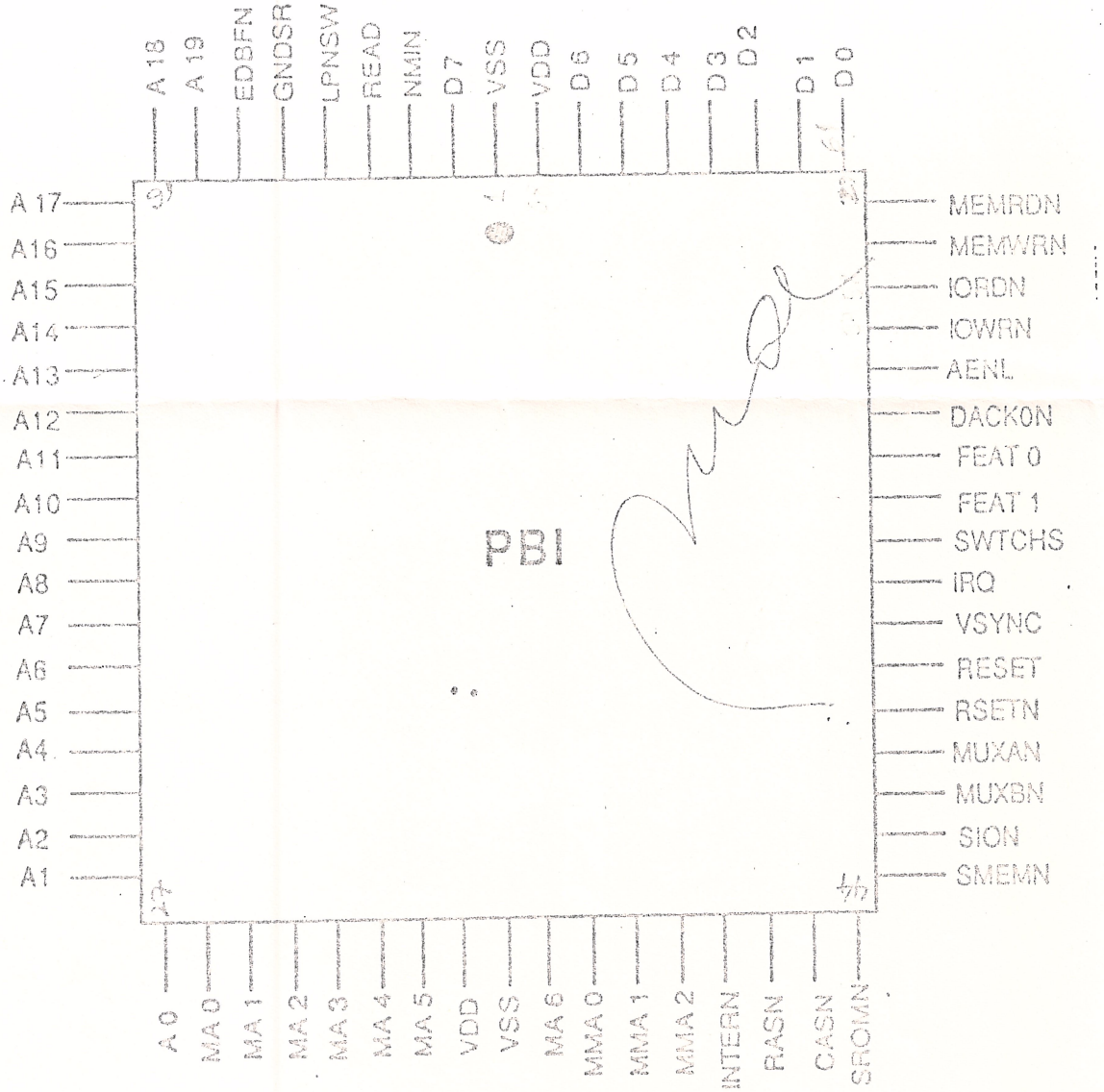
*/A8*A7*A6*A5*/A4*/IOR+/AEN*/A9*/A8*A7*A6*A5*/A4*/IOW

DESCRIPTION

The Paradise Bus Interface chip (PBI) is a 2 micron, 1400 gate companion to the popular Paradise PEGA series of gate array and standard cell devices. Using this 68 pin, PLCC, Paradise OEM customers can implement an EGA based multi-mode, AutoSwitch™ video design with a total package count of 14.

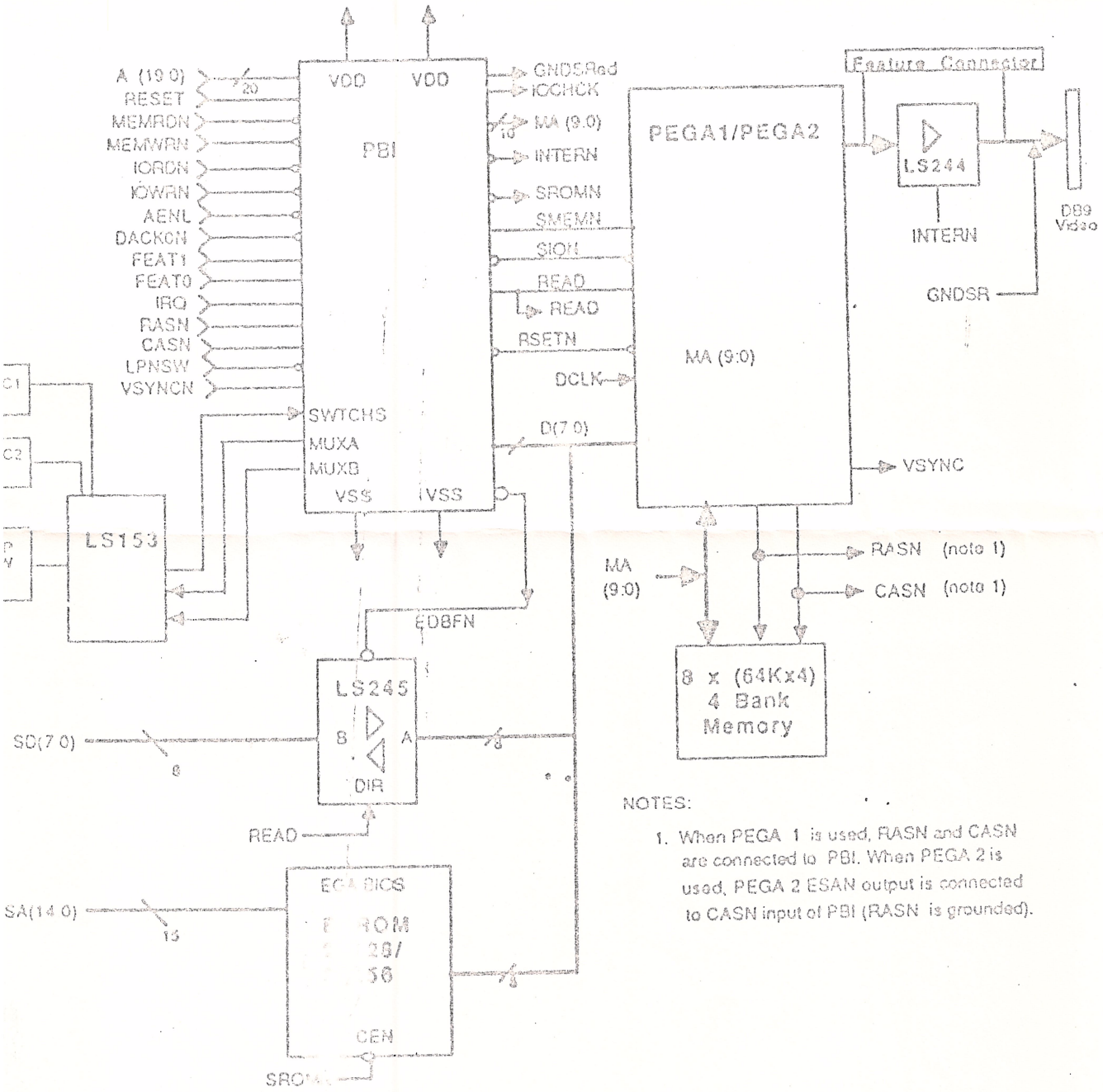
This device adds to the current PEGA 1 or 2 repertoire of features:

- Optional automatic BIOS ROM disable in 6845 modes.
- PEGA register data may be read back from PBI "shadow" registers



NOTES:

1. ● = PIN 1. PIN NUMBERS INCREASE COUNTERCLOCKWISE.
2. PACKAGE IS 68 PIN PLCC.



NOTES:

1. When PEGA 1 is used, RASN and CASN are connected to PBI. When PEGA 2 is used, PEGA 2 ESAN output is connected to CASN input of PBI (RASN is grounded).

ABSOLUTE MAXIMUM RATINGS

Ambient temperature under bias	0° C to 70° C
Storage temperature	-40° C to 100° C
Voltage on all inputs and outputs with respect to V_{SS}	-0.5 to 7 Volts
Power Dissapation	1.0 Watt

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

DESCRIPTION OF PBI SIGNALS
(pin number in brackets)

D(7:0) [2,68-61]	I/O	Input for buffered system data bits 0 to 7. Output for multiplexed system address 0 to 5 ans 15, 16.
NMIN[3]	Output	- Active low, I/O channel check.
INTERN[40]	Output	- Active low, Video buffer enable.
SROMN[43]	Output	- Active low, ROM BIOS enable signal.
SION[45]	Output	- Active low, PEGA I/O selected.
SMEM[44]	Output	- Active low, video memory selected
READ[4]	Output	- Active high, read PEGA I/O port or video memory
RSETN[48]	Output	- Active low, master reset.
EDBEN[7]	Output	- Active low, memory or I/O selected, enables ext data bus driver.
GNDSR[6]	Output	- Active high, ground secondary red.
MUX A[47], MUX B[46]	Outputs	- Select switch status and clock speed.
SA (19:0) [8-27]	Inputs	Systems address bits 0 to 19
MEMRDN [60]	Input	Active low, memory read.
MEMWRN [59]	Input	Active low, memory write.
IORDN[58]	Input	- Active low, I/O read.
IOWRN[57]	Input	- Active low, I/O write.

AENL[56]	Input	- DMA Controller has control of address, data and control buses when active (high).
DACK0N[55]	Input	- Active low, DMA acknowlege 0, to refresh system DRAMS.
FEAT1[53], FEAT0[54]	Inputs	- Feature connecture status bits 1 and 0.
IRQ[51]	Input	- Interrupt 2 generated by PEGA.
LPNSW[5]	Input	- Used for light pen switch input.
RASN[41]	Input	- Input for RASN from PEGA 1, ground for PEGA 2.
CASN/ESAN [42]	Input	- Input for CASN from PEGA 1, ESAN from PEGA 2.
SWTCHS [52]	Input	- Switch status input controlled by MUX A and MUX B.
VSYNC[50]	Input	- Vertical sync from PEGA (required for Autoswitch Here. mode only).

PBI Control register description:

Address	Bit	Function
3DF		Write only reg.
	D7=0	ROM BIOS active
	D7=1	ROM BIOS mapped out
	D6=0	Video DRAM mapped normally
	D6=1	Video DRAM and PEGA chip I/O read mapped out, shadow RAM mapped in.
	D5=0	External scratch pad RAM mapped out
	D5=1	External scratch pad RAM mapped in. Note 1
	D4=0	Reserved, must be programmed to 0 at all times.
	D3=0	PBI connected to PEGA2
	D3=1	PBI connected to PEGA1
	D2=0	No NMI
	D2=1	NMI 2: Caused by IOW to 3BF,3D9,3DD,3DE
	D1=0	No NMI
	D1=1	NMI 1: Caused by IOW to 3x8
	D0=0	No NMI
	D0=1	NMI 0: Caused by IOW to 3x5 (CRTC)
CONFIG.		This register is write only and is loaded during RESET active and latched when RESET goes inactive. Note 2
	MA0=0	IO ports mapped as 2xx
	MA0=1	IO ports mapped as 3xx (standard condition)
	MA1=0	32K BIOS installed
	MA1=1	16K BIOS installed (standard condition)
	MA2 through MA6	Software definable and read through port 3XA
3DD 3DE		This register is read only. It is accessed with a IOR if NMI 1,2,or 0 is enabled and 3DF:D6=1. See note page.
	3DD BITS 4-7	Contains 1's compliment of I/O index address
	3DD BITS 0-3	Contains 1's compliment of I/O address causing NMI
	3DE bits 0-7	Data associated with IOW causing NMI

Notes:

1. The config. register inputs are preset for latching by using 4.7k ohm pullup or pulldown resistors on the appropriate MA0 through MA6 lines.

2. PEGA registers can be read at the I/O address if 3DF-bit 6 is set to 1. The registers saved are 3C0,3C2, 3DF,3X4,3X8,3XA,3DF-Q0,Q1,Q2.

   3DF-Q1,Q2,Q3 are cleared by MW to 0000B through 0000B.

3. There are seven bytes of scratch RAM available at A000 segment offset at 3C4,3CA,3CB,3CC,3CD,3CE,3CF. This RAM is accessed by a Memrd or Memwr if 3DF-bit 6 is set to 1.