

## MANUAL DE CI's 1



8272A

During the Command Phase of the Seek operation the FDC is in the FDC BUSY state, but during the Execution Phase it is in the NON BUSY state. While the FDC is in the NON BUSY state, another Seek Command may be issued, and in this manner parallel seek operations may be done on up to 4 Drives at once.

If an FDD is in a NOT READY state at the beginning of the command execution phase or during the seek operation, then the NR (NOT READY) flag is set in Status Register 0 to a 1 (high), and the command is terminated.

Note that the 8272A Read and Write Commands do not have implied Seeks. Any R/W command should be preceded by: 1) Seek Command; 2) Sense Interrupt Status; and 3) Read ID.

#### RECALIBRATE

This command causes the read/write head within the FDD to retract to the Track 0 position. The FDC clears the contents of the PCN counter, and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is low, the Direction signal remains 1 (high) and Step Pulses are issued. When the Track 0 signal goes high, the SE (SEEK END) flag in Status Register 0 is set to a 1 (high) and the command is terminated. If the Track 0 signal is still low after 77 Step Pulses have been issued, the FDC sets the SE (SEEK END) and EC (EQUIPMENT CHECK) flags of Status Register 0 to both 1s (highs), and terminates the command.

The ability to overlap RECALIBRATE Commands to multiple FDDs, and the loss of the READY signal, as described in the SEEK Command, also applies to the RECALIBRATE Command.

#### SENSE INTERRUPT STATUS

An interrupt signal is generated by the FDC for one of the following reasons:

1. Upon entering the Result Phase of:
  - a. Read Data Command
  - b. Read a Track Command
  - c. Read ID Command
  - d. Read Deleted Data Command
  - e. Write Data Command
  - f. Format a Cylinder Command
  - g. Write Deleted Data Command
  - h. Scan Commands
2. Ready Line of FDD changes state
3. End of Seek or Recalibrate Command
4. During Execution Phase in the NON-DMA Mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. However, interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status Command. This command when issued resets the interrupt signal and via bits 5, 6, and 7 of Status Register 0 identifies the cause of the interrupt.

Neither the Seek or Recalibrate Command have a Result Phase. Therefore, it is mandatory to use the Sense Interrupt Status Command after these commands to effectively terminate them and to provide verification of the head position (PCN).

Table 11. Seek, Interrupt Codes

SEEK END BIT 5	INTERRUPT CODE		CAUSE
	BIT 6	BIT 7	
0	1	1	Ready Line changed state, either polarity
1	0	0	Normal Termination of Seek or Recalibrate Command
1	1	0	Abnormal Termination of Seek or Recalibrate Command

#### SPECIFY

The Specify Command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution Phase of one of the Read/Write Commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (01 = 16 ms, 02 = 32 ms, ..., 0F = 240 ms). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and when the Read/Write operation starts. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms, ..., FE = 254 ms).

The step rate should be programmed 1 mS longer than the minimum time required by the drive.

The time intervals mentioned above are a direct function of the clock (CLK on pin 19). Times indicated above are for an 8 MHz clock, if the clock was reduced to 4 MHz (mini-floppy application) then all time intervals are increased by a factor of 2.

The choice of DMA or NON-DMA operation is made by the ND (NON-DMA) bit. When this bit is high (ND = 1) the NON-DMA mode is selected, and when ND = 0 the DMA mode is selected.

#### SENSE DRIVE STATUS

This command may be used by the processor whenever it wishes to obtain the status of the FDDs. Status Register 3 contains the Drive Status information.

#### INVALID

If an invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command. No interrupt is generated by the 8272A during this condition. Bit 6 and bit 7 (DIO and RQM) in the Main Status Register are both high ("1") indicating to the processor that the 8272A is in the Result Phase and the contents of Status Register 0 (ST0) must be read. When the processor reads Status Register 0 it will find an 80H indicating an invalid command was received.

A Sense Interrupt Status Command must be sent after a Seek or Recalibrate interrupt, otherwise the FDC will consider the next command to be an Invalid Command.

In some applications the user may wish to use this command as a No-Op command, to place the FDC in a stand-by or no operation state.





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Table 12. Status Registers

BIT			DESCRIPTION
NO.	NAME	SYMBOL	
STATUS REGISTER 0			
D <sub>7</sub>	Interrupt Code	IC	D <sub>7</sub> = 0 and D <sub>6</sub> = 0 Normal Termination of Command, (NT). Command was completed and properly executed.
D <sub>6</sub>			D <sub>7</sub> = 0 and D <sub>6</sub> = 1 Abnormal Termination of Command, (AT). Execution of Command was started, but was not successfully completed.
			D <sub>7</sub> = 1 and D <sub>6</sub> = 0 Invalid Command Issue, (IC). Command which was issued was never started.
			D <sub>7</sub> = 1 and D <sub>6</sub> = 1 Abnormal Termination because during command execution the ready signal from FDD changed state.
D <sub>5</sub>	Seek End	SE	When the FDC completes the SEEK Command, this flag is set to 1 (high).
D <sub>4</sub>	Equipment Check	EC	If a fault Signal is received from the FDD, or if the Track 0 Signal fails to occur after 77 Step Pulses (Recalibrate Command) then this flag is set.
D <sub>3</sub>	Not Ready	NR	When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to Side 1 of a single sided drive, then this flag is set.
D <sub>2</sub>	Head Address	HD	This flag is used to indicate the state of the head at Interrupt.
D <sub>1</sub>	Unit Select 1	US 1	These flags are used to indicate a Drive Unit Number at Interrupt
D <sub>0</sub>	Unit Select 0	US 0	
STATUS REGISTER 1			
D <sub>7</sub>	End of Cylinder	EN	When the FDC tries to access a Sector beyond the final Sector of a Cylinder, this flag is set.
D <sub>6</sub>			Not used. This bit is always 0 (low).
D <sub>5</sub>	Data Error	DE	When the FDC detects a CRC error in either the ID field or the data field, this flag is set.
D <sub>4</sub>	Over Run	OR	If the FDC is not serviced by the main-systems during data transfers, within a certain time interval, this flag is set.
D <sub>3</sub>			Not used. This bit always 0 (low).
D <sub>2</sub>	No Data	ND	During execution of READ DATA, WRITE DELETED DATA or SCAN Command, if the FDC cannot find the Sector specified in the IDR Register, this flag is set.
			During executing the READ ID Command, if the FDC cannot read the ID field without an error, then this flag is set.
			During the execution of the READ A Cylinder Command, if the starting sector cannot be found, then this flag is set.

BIT			DESCRIPTION
NO.	NAME	SYMBOL	
STATUS REGISTER 1 (CONT.)			
D <sub>1</sub>	Not Writable	NW	During execution of WRITE DATA, WRITE DELETED DATA or Format A Cylinder Command, if the FDC detects a write protect signal from the FDD, then this flag is set.
D <sub>0</sub>	Missing Address Mark	MA	If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set.  If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. Also at the same time, the MD (Missing Address Mark in Data Field) of Status Register 2 is set.
STATUS REGISTER 2			
D <sub>7</sub>			Not used. This bit is always 0 (low).
D <sub>6</sub>	Control Mark	CM	During executing the READ DATA or SCAN Command, if the FDC encounters a Sector which contains a Deleted Data Address Mark, this flag is set.
D <sub>5</sub>	Data Error in Data Field	DD	If the FDC detects a CRC error in the data field then this flag is set.
D <sub>4</sub>	Wrong Cylinder	WC	This bit is related with the ND bit, and when the contents of C on the medium is different from that stored in the IDR, this flag is set.
D <sub>3</sub>	Scan Equal Hit	SH	During execution, the SCAN Command, if the condition of "equal" is satisfied, this flag is set.
D <sub>2</sub>	Scan Not Satisfied	SN	During executing the SCAN Command, if the FDC cannot find a Sector on the cylinder which meets the condition, then this flag is set.
D <sub>1</sub>	Bad Cylinder	BC	This bit is related with the ND bit, and when the content of C on the medium is different from that stored in the IDR and the content of C is FF, then this flag is set.
D <sub>0</sub>	Missing Address Mark in Data Field	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set.
STATUS REGISTER 3			
D <sub>7</sub>	Fault	FT	This bit is used to indicate the status of the Fault signal from the FDD.
D <sub>6</sub>	Write Protected	WP	This bit is used to indicate the status of the Write Protected signal from the FDD.
D <sub>5</sub>	Ready	RDY	This bit is used to indicate the status of the Ready signal from the FDD.
D <sub>4</sub>	Track 0	T0	This bit is used to indicate the status of the Track 0 signal from the FDD.
D <sub>3</sub>	Two Side	TS	This bit is used to indicate the status of the Two Side signal from the FDD.
D <sub>2</sub>	Head Address	HD	This bit is used to indicate the status of Side Select signal to the FDD.
D <sub>1</sub>	Unit Select 1	US 1	This bit is used to indicate the status of the Unit Select 1 signal to the FDD.
D <sub>0</sub>	Unit Select 0	US 0	This bit is used to indicate the status of the Unit Select 0 signal to the FDD.

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## ABSOLUTE MAXIMUM RATINGS\*

Operating Temperature ..... 0°C to +70°C  
 Storage Temperature ..... -40°C to +125°C  
 All Output Voltages ..... -0.5 to +7 Volts  
 All Input Voltages ..... -0.5 to +7 Volts  
 Supply Voltage  $V_{CC}$  ..... -0.5 to +7 Volts  
 Power Dissipation ..... 1 Watt

\* $T_A = 25^\circ\text{C}$ 

NOTICE: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS ( $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = +5\text{V} \pm 10\%$ )

Symbol	Parameter	Limits		Unit	Test Conditions
		Min.	Max.		
$V_{IL}$	Input Low Voltage	-0.5	0.8	V	
$-V_{IH}$	Input High Voltage	2.0	$V_{CC} + 0.5$	V	
$V_{OL}$	Output Low Voltage		0.45	V	$I_{OL} = 2.0\text{ mA}$
$V_{OH}$	Output High Voltage	2.4	$V_{CC}$	V	$I_{OH} = -400\text{ }\mu\text{A}$
$I_{CC}$	$V_{CC}$ Supply Current		120	mA	
$I_{IL}$	Input Load Current (All Input Pins)		10 -10	$\mu\text{A}$ $\mu\text{A}$	$V_{IN} = V_{CC}$ $V_{IN} = 0\text{V}$
$I_{LOH}$	High Level Output Leakage Current		10	$\mu\text{A}$	$V_{OUT} = V_{CC}$
$I_{OFL}$	Output Float Leakage Current		$\pm 10$	$\mu\text{A}$	$0.45\text{V} \leq V_{OUT} \leq V_{CC}$

CAPACITANCE ( $T_A = 25^\circ\text{C}$ ,  $f_c = 1\text{ MHz}$ ,  $V_{CC} = 0\text{V}$ )

Symbol	Parameter	Limits		Unit	Test Conditions
		Min.	Max.		
$C_{IN(e)}$	Clock Input Capacitance		20	pF	All Pins Except Pin Under Test Tied to AC Ground
$C_{IN}$	Input Capacitance		10	pF	
$C_{IO}$	Input/Output Capacitance		20	pF	

A.C. CHARACTERISTICS ( $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = +5.0\text{V} \pm 10\%$ )

## CLOCK TIMING

Symbol	Parameter	Min.	Max.	Unit	Notes
$t_{CY}$	Clock Period	120	500	ns	Note 5
$t_{CH}$	Clock High Period	40		ns	Note 4, 5
$t_{RST}$	Reset Width	14		tCY	

## READ CYCLE

$t_{AR}$	Select Setup to $\overline{RD}$	0		ns	
$t_{RA}$	Select Hold from $\overline{RD}$	0		ns	
$t_{RR}$	$\overline{RD}$ Pulse Width	250		ns	
$t_{RD}$	Data Delay from $\overline{RD}$		200	ns	
$t_{DF}$	Output Float Delay	20	100	ns	



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A.C. CHARACTERISTICS (Continued) ( $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = +5.0\text{V} \pm 10\%$ )

WRITE CYCLE						
Symbol	Parameter	Typ.1	Min.	Max.	Unit	Notes
$t_{AW}$	Select Setup to $\overline{WR}^\dagger$		0		ns	
$t_{WA}$	Select Hold from $\overline{WR}^\dagger$		0		ns	
$t_{WW}$	$\overline{WR}$ Pulse Width		250		ns	
$t_{DW}$	Data Setup to $\overline{WR}^\dagger$		150		ns	
$t_{WD}$	Data Hold from $\overline{WR}^\dagger$		5		ns	
INTERRUPTS						
$t_{RI}$	INT Delay from $\overline{RD}^\dagger$			500	ns	Note 6
$t_{WI}$	INT Delay from $\overline{WR}^\dagger$			500	ns	Note 6
DMA						
$t_{ROCY}$	DRQ Cycle Period		13		$\mu\text{s}$	Note 6
$t_{AKRO}$	$\overline{DACK}_i$ to $\overline{DRQ}_i$			200	ns	
$t_{ROR}$	$\overline{DRQ}_i$ to $\overline{RD}_i$		800		ns	Note 6
$t_{ROW}$	$\overline{DRQ}_i$ to $\overline{WR}_i$		250		ns	Note 6
$t_{RORW}$	$\overline{DRQ}_i$ to $\overline{RD}_i$ or $\overline{WR}_i$			12	$\mu\text{s}$	Note 6
FDD INTERFACE						
$t_{WCY}$	WCK Cycle Time	2 or 4 1 or 2			$\mu\text{s}$	MFM = 0 MFM = 1 Note 2
$t_{WCH}$	WCK High Time	250	80	350	ns	
$t_{CP}$	Pre-Shift Delay from WCK $^\dagger$		20	100	ns	
$t_{CD}$	WDA Delay from WCK $^\dagger$		20	100	ns	
$t_{WDD}$	Write Data Width		$t_{WCH} - 50$		ns	
$t_{WE}$	$\overline{WE}_i$ to WCK $^\dagger$ or $\overline{WE}_i$ to WCK $^\dagger$ Delay		20	100	ns	
$t_{WWCY}$	Window Cycle Time	2 1			$\mu\text{s}$	MFM = 0 MFM = 1
$t_{WRD}$	Window Setup to $\overline{RDD}_i$		15		ns	
$t_{RDW}$	Window Hold from $\overline{RDD}_i$		15		ns	
$t_{RDD}$	$\overline{RDD}$ Active Time (HIGH)		40		ns	
FDD SEEK/DIRECTION/STEP						
$t_{US}$	$\overline{US}_{0,1}$ Setup to $\overline{RW}/\text{SEEK}^\dagger$		12		$\mu\text{s}$	Note 6
$t_{SU}$	$\overline{US}_{0,1}$ Hold after $\overline{RW}/\text{SEEK}^\dagger$		15		$\mu\text{s}$	Note 6
$t_{SD}$	$\overline{RW}/\text{SEEK}$ Setup to LCT/DIR		7		$\mu\text{s}$	Note 6
$t_{DS}$	$\overline{RW}/\text{SEEK}$ Hold from LCT/DIR		30		$\mu\text{s}$	Note 6
$t_{DST}$	LCT/DIR Setup to FR/STEP $^\dagger$		1		$\mu\text{s}$	Note 6
$t_{STD}$	LCT/DIR Hold from FR/STEP $^\dagger$		24		$\mu\text{s}$	Note 6
$t_{STU}$	$\overline{DS}_{2,1}$ Hold from FR/STEP $^\dagger$		5		$\mu\text{s}$	Note 6
$t_{STP}$	STEP Active Time (High)	5			$\mu\text{s}$	Note 6
$t_{SC}$	STEP Cycle Time		33		$\mu\text{s}$	Note 3, 6
$t_{FR}$	FAULT RESET Active Time (High)		8	10	$\mu\text{s}$	Note 6
$t_{IDX}$	INDEX Pulse Width	10			tCY	
$t_{TC}$	Terminal Count Width		1		tCY	

## NOTES:

1. Typical values for  $T_A = 25^\circ\text{C}$  and nominal supply voltage.
2. The former values are used for standard floppy and the latter values are used for mini-floppies.
3.  $t_{SC} = 33 \mu\text{s}$  min. is for different drive units. In the case of same unit,  $t_{SC}$  can be ranged from 1 ms to 16 ms with 8 MHz clock period, and 2 ms to 32 ms with 4 MHz clock, under software control.
4. From 2.0V to +2.0V.
5. At 4 MHz, the clock duty cycle may range from 16% to 76%. Using an 8 MHz clock the duty cycle can range from 32% to 52%. Duty cycle is defined as: D.C. =  $100(t_{CH} + t_{CY})$  with typical rise and fall times of 5 ns.
6. The specified values listed are for an 8 MHz clock period. Multiply timings by 2 when using a 4 MHz clock period.

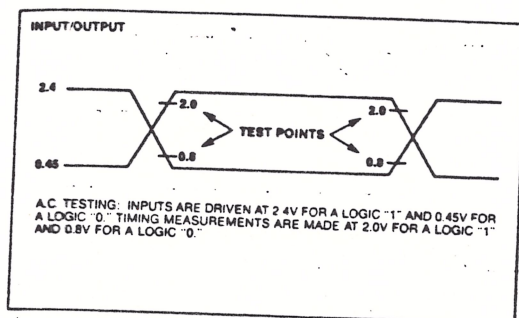


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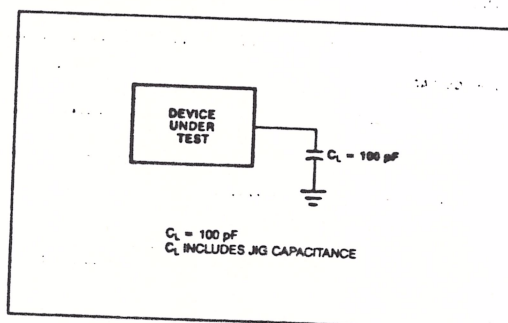
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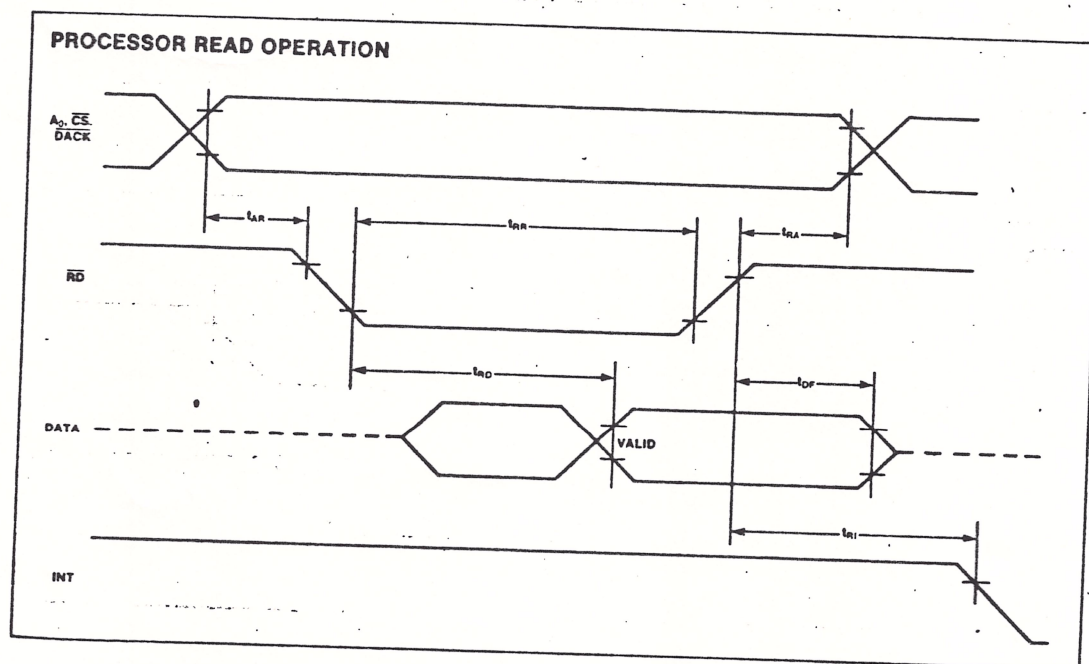
## A.C. TESTING INPUT, OUTPUT WAVEFORM



## A.C. TESTING LOAD CIRCUIT



## WAVEFORMS

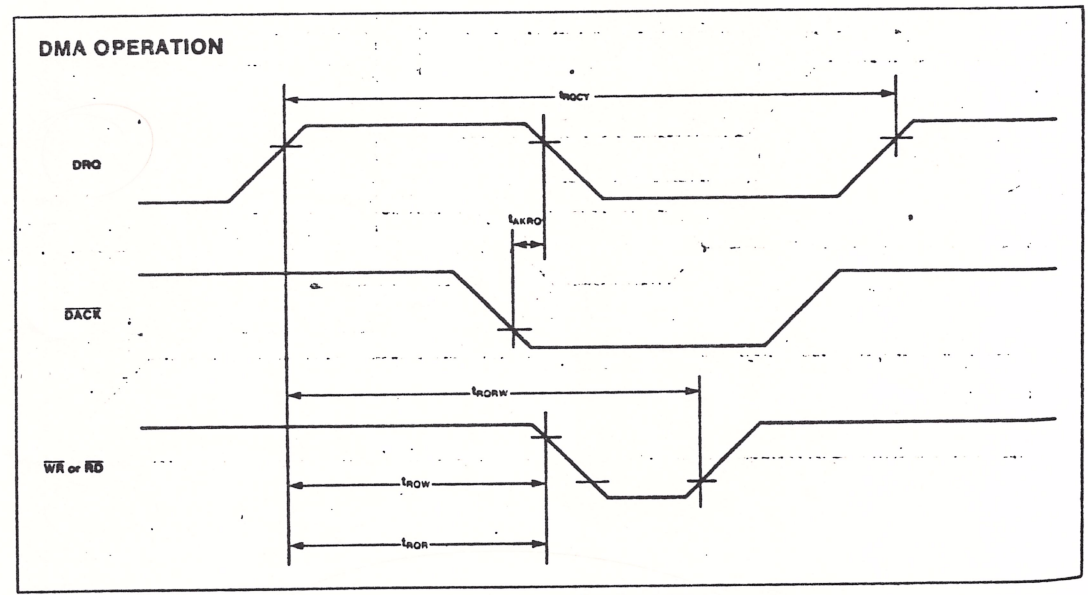
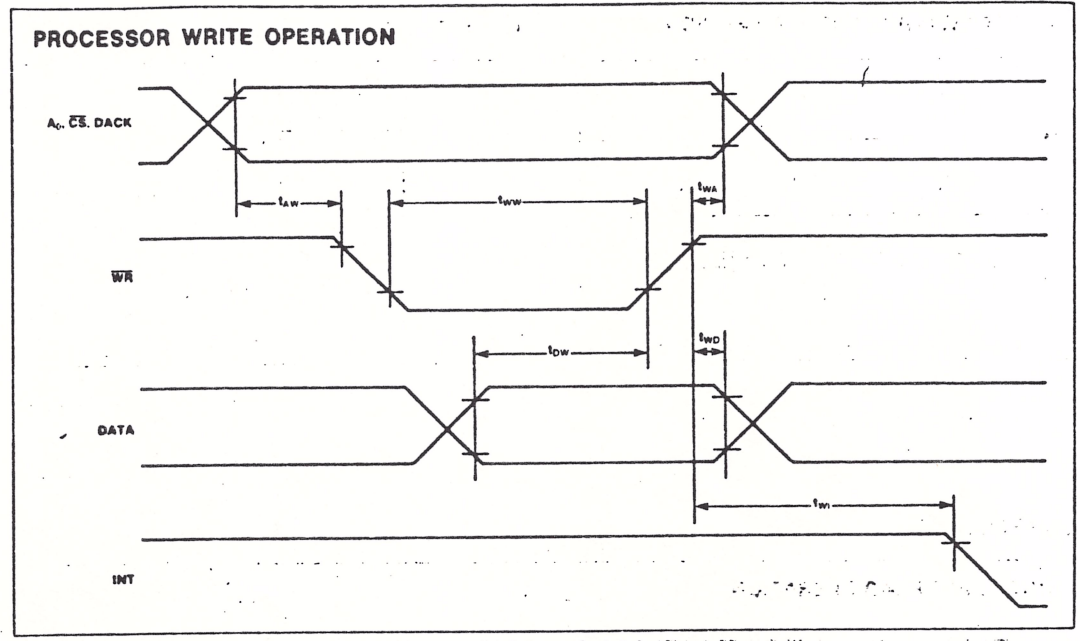


6 clk  $\rightarrow$   $1.2 \mu s$



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WAVEFORMS (Continued)



$13 \mu s \rightarrow DRQ$



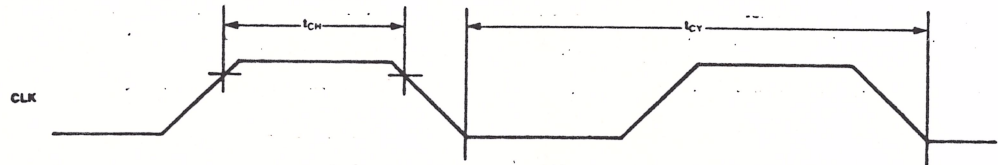
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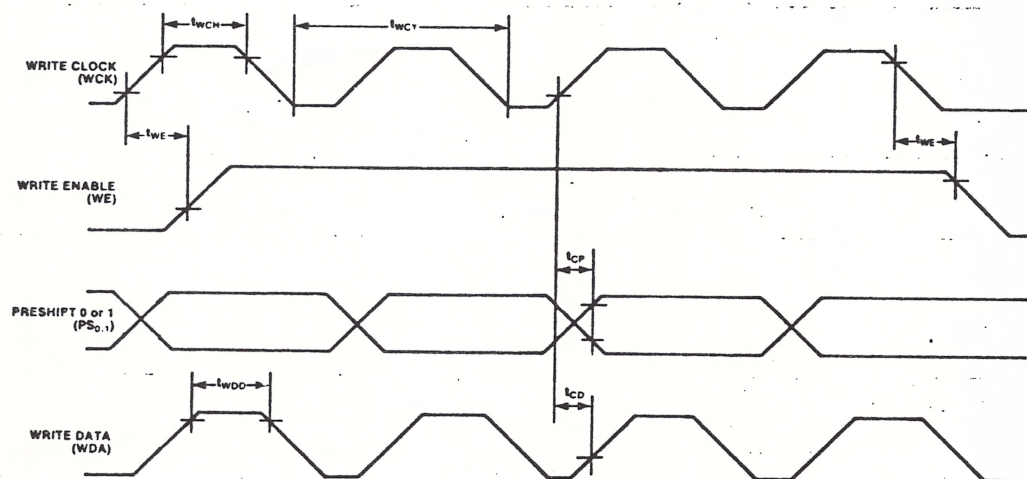
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## WAVEFORMS (Continued)

## CLOCK TIMING



## FDD WRITE OPERATION

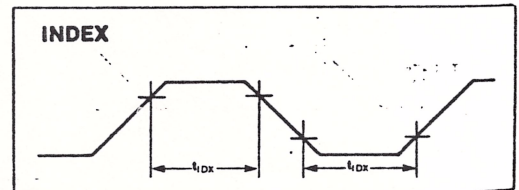
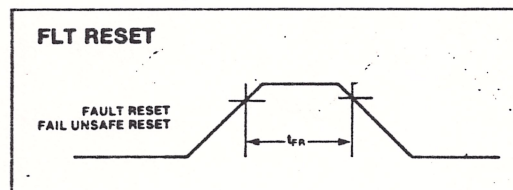
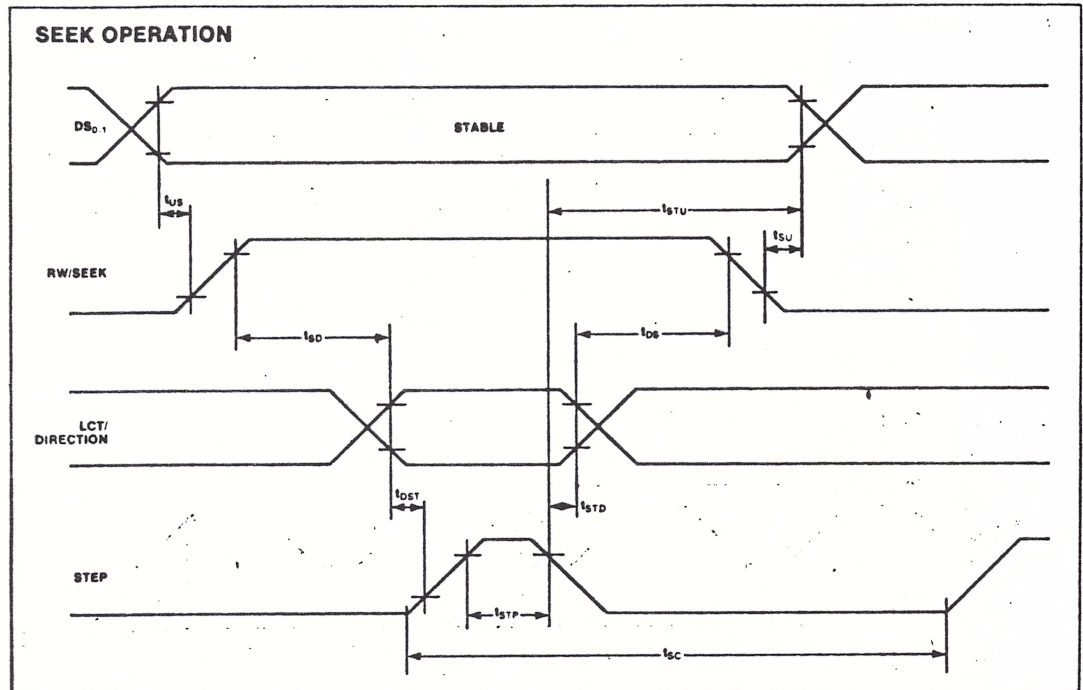


	PRESIFT 0	PRESIFT 1
NORMAL	0	0
LATE	0	1
EARLY	1	0
INVALID	1	1

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## WAVEFORMS (Continued)





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## WAVEFORMS (Continued)

